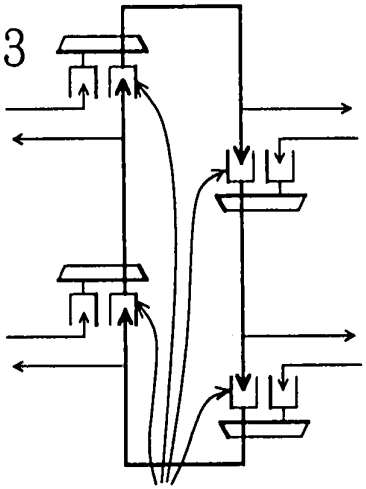
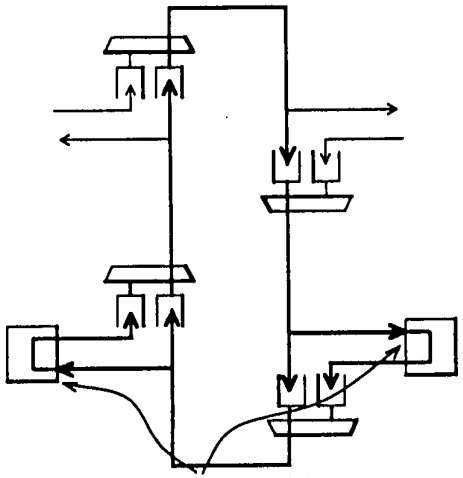
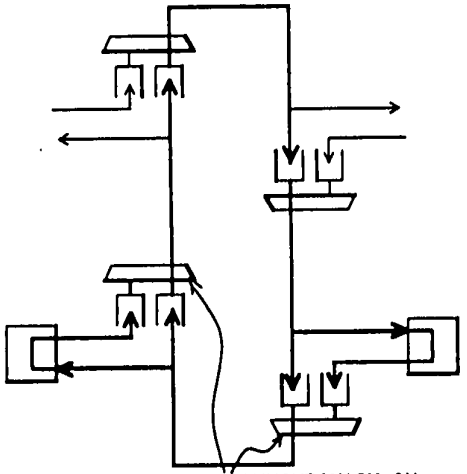
FIG.23



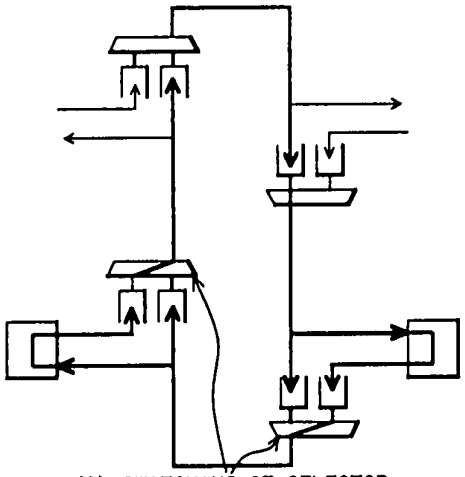
FIXED DELAY NEEDED FOR PREDETERMINED OPERATION
(a) INITIAL STATE



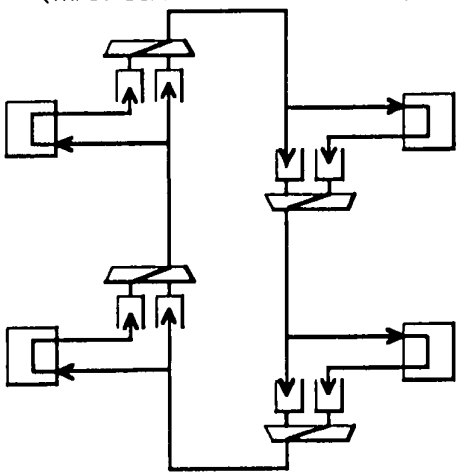
(1) ESTABLISH SYNCHRONISM ON INPUT BUFFER SIDE
(b) EXTENSION (INPUT BUFFER SYNCHRONIZATION)



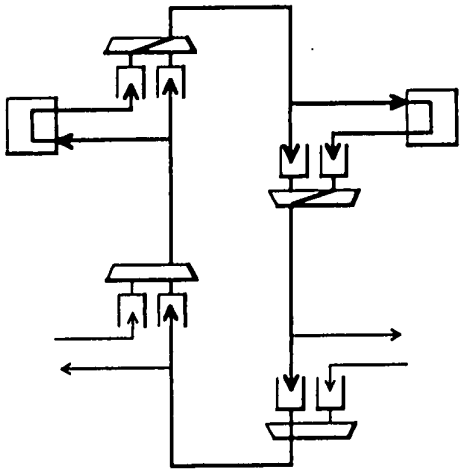
(2) ESTABLISH SYNCHRONISM ON BYPASS SWITCH SIDE
(c) EXTENSION (BYPASS SWITCH SYNCHRONIZATION)



(3) SWITCHING OF SELECTOR
(d) START OF OPERATION



(e) EXTENSION



(f) REPLACEMENT

FIG.24

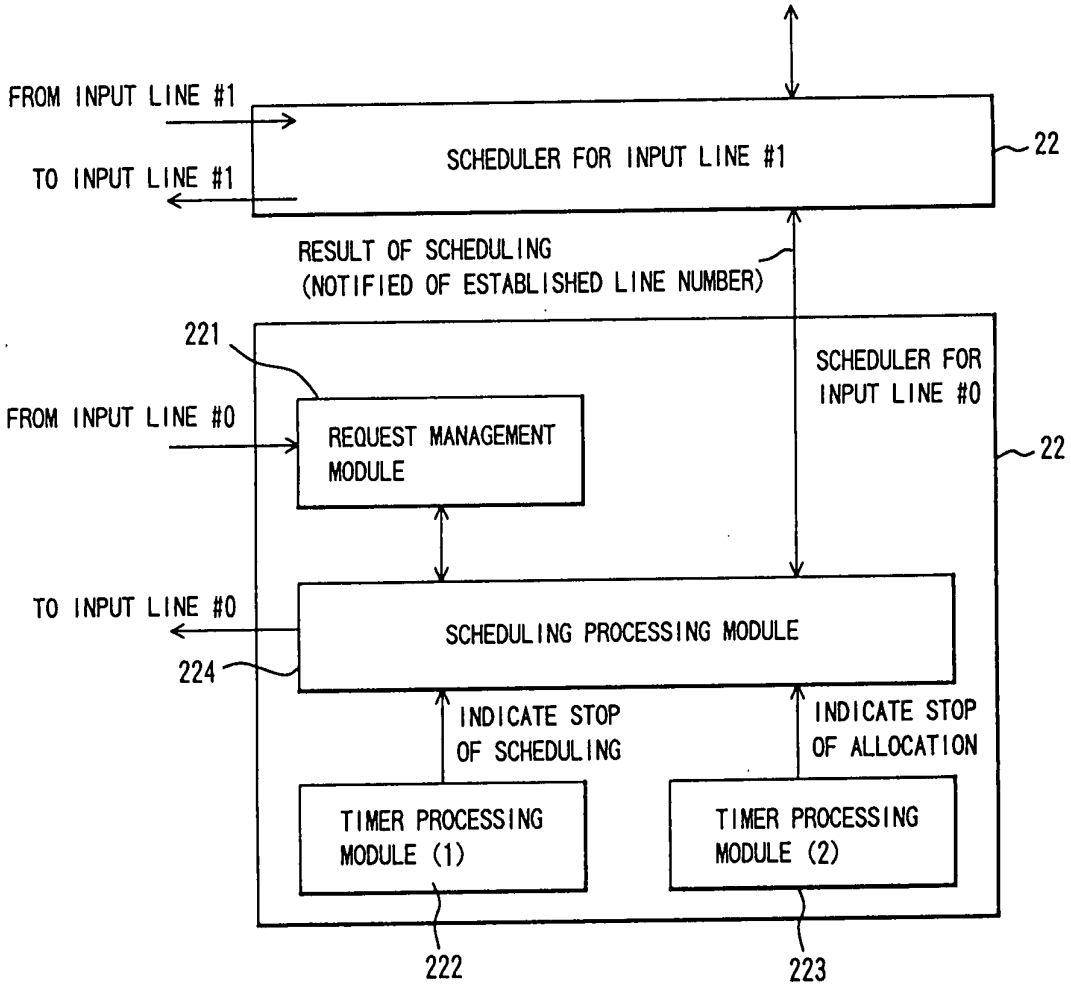

FROM INPUT LINE #1
TO INPUT LINE #1
SCHEDULER FOR INPUT LINE #1
22
RESULT OF SCHEDULING
(NOTIFIED OF ESTABLISHED LINE NUMBER)
221
FROM INPUT LINE #0
REQUEST MANAGEMENT MODULE
SCHEDULER FOR INPUT LINE #0
22
TO INPUT LINE #0
SCHEDULING PROCESSING MODULE
224
INDICATE STOP OF SCHEDULING
INDICATE STOP OF ALLOCATION
TIMER PROCESSING MODULE (1)
TIMER PROCESSING MODULE (2)
222
223

FIG.25

```
-- ACQUISITION OF ADDRESS
   IF INI_CNT < MAX          -- ACQUIRED FROM ADDRESS GENERATION COUNTER
          INI_CNT ++
          W_ADR = INT_CNT
   ELSE                      -- ACQUIRED FROM FREE ADDRESS FIFO
          W_ADR = EMP_S_PNT
          EMP_S_PNT = LINK(EMP_S_PNT)
   ENDIF
-- UPDATING OF POINTER LINK

   IF CNT_L(BUF) = 0         -- PROCESSING WHEN CELL BUFFER IS FREE

          S_PNT(BUF) = W_ADR
          E_PNT(BUF) = W_ADR
   ELSE                    -- PROCESSING WHEN CELL BUFFER IS NOT FREE

          LINK(E_PNT(BUF)) = W_ADR
          E_PNT(BUF) = W_ADR

   ENDIF

-- UPDATING OF COUNTER

   CNT_L(BUF) ++
   CNT_S(QOS) ++

-- UPDATING OF BUFFER ADDRESS
   BUF_A(W_ADR) <= W_ADR

-- UPDATING OF BITMAP
   IF CELL(M) = 0            -- CASE OF UNICAST CELL

             BMAP(W_ADR) <= BITMAP(CELL(UC-TAG))
   ELSE                      -- CASE OF MULTICAST CELL

             BMAP(W_ADR) <= CELL(MC-TAG))
   ENDIF
```

```
INI_CNT:   INITIAL ADDRESS GENERATION COUNTER
MAX:       BUFFER LENGTH IN USE
W_ADR:     WRITE ADDRESS
EMP_S_PNT:FREE ADDRESS FIFO START POINTER
LINK(x):   ADDRESS LINKED TO ADDRESS x
CNT_L(x):  INDIVIDUAL BUFFER QUEUE LENGTH OF BUFFER x
CNT_M(x):  MULTICAST BUFFER QUEUE LENGTH OF QoS CLASS x
CNT_S(x):  COMMON BUFFER QUEUE LENGTH OF QoS CLASS x
S_PNT(x):  START POINTER OF BUFFER x
E_PNT(x):  END POINTER OF BUFFER x
BUF_A(x):  BUFFER ADDRESS OF ADDRESS x
CELL(x):   VALUE OF HEADER x OF INPUT CELL
BMAP(x):   ROUTING BIT (BITMAP) OF ADDRESS x
BITMAP(x):CONVERT CODE x INTO BITMAP
```

FIG.26

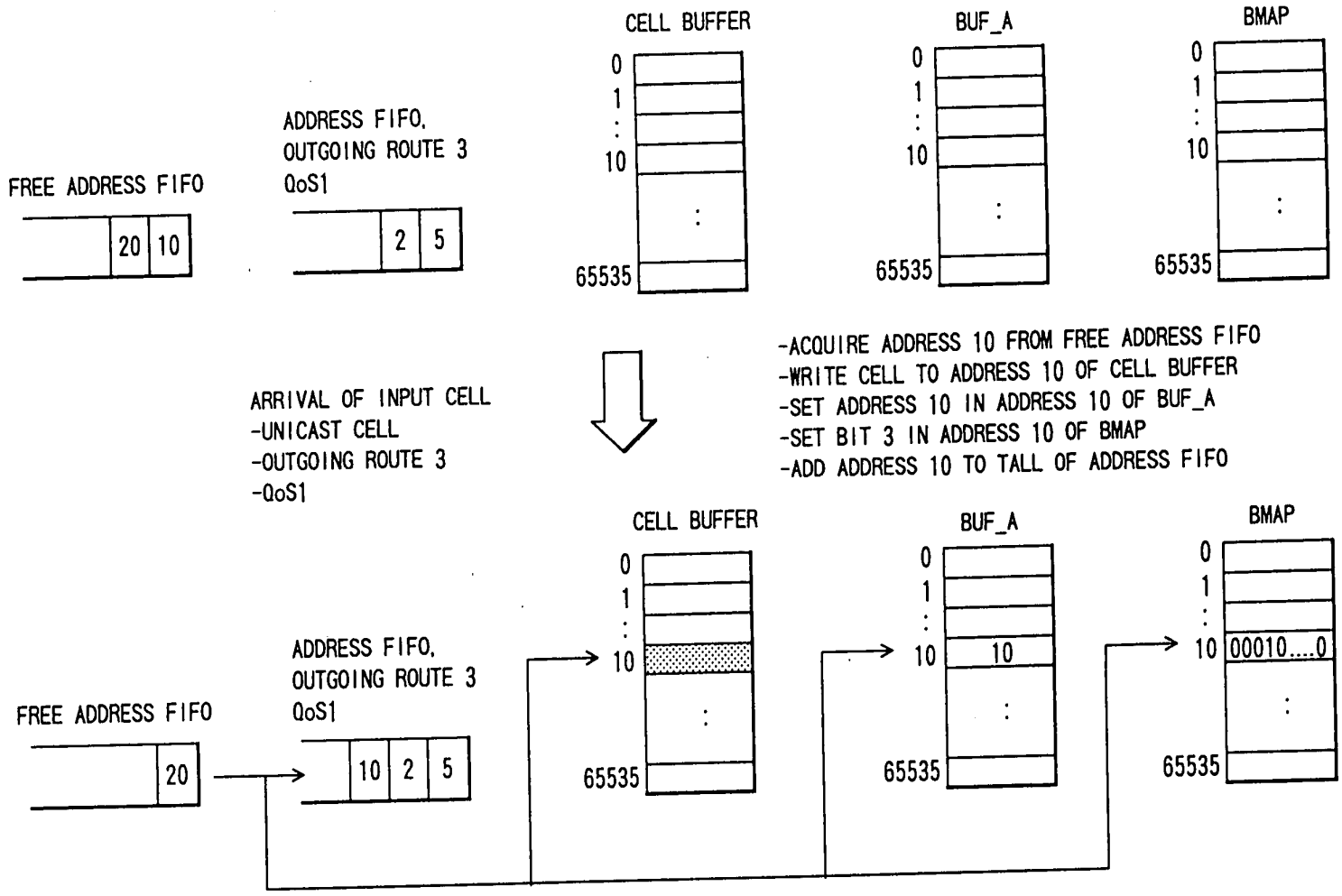

CELL BUFFER
BUF_A
BMAP
FREE ADDRESS FIFO
20
10
ADDRESS FIFO,
OUTGOING ROUTE 3
QoS1
2
5
0
1
10
65535
ARRIVAL OF INPUT CELL
-UNICAST CELL
-OUTGOING ROUTE 3
-QoS1
-ACQUIRE ADDRESS 10 FROM FREE ADDRESS FIFO
-WRITE CELL TO ADDRESS 10 OF CELL BUFFER
-SET ADDRESS 10 IN ADDRESS 10 OF BUF_A
-SET BIT 3 IN ADDRESS 10 OF BMAP
-ADD ADDRESS 10 TO TALL OF ADDRESS FIFO
00010....0

FIG.27

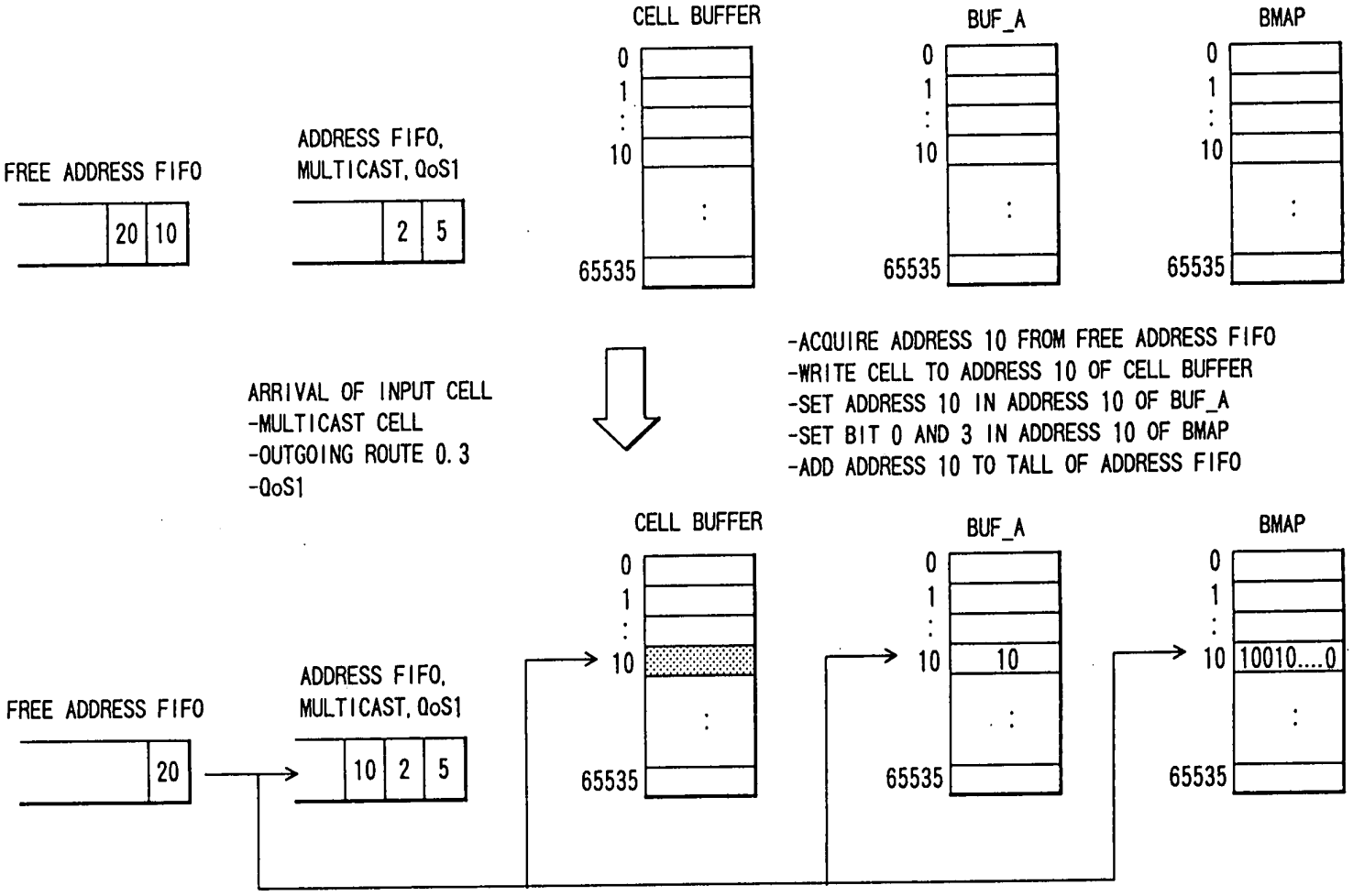

CELL BUFFER
BUF_A
BMAP
FREE ADDRESS FIFO
ADDRESS FIFO, MULTICAST, QoS1
20
10
2
5
0
1
10
65535
ARRIVAL OF INPUT CELL
-MULTICAST CELL
-OUTGOING ROUTE 0.3
-QoS1
-ACQUIRE ADDRESS 10 FROM FREE ADDRESS FIFO
-WRITE CELL TO ADDRESS 10 OF CELL BUFFER
-SET ADDRESS 10 IN ADDRESS 10 OF BUF_A
-SET BIT 0 AND 3 IN ADDRESS 10 OF BMAP
-ADD ADDRESS 10 TO TALL OF ADDRESS FIFO
10010....0

FIG.28

```
-- ACQUISITION OF ADDRESS
    IF MC_TOP E = 0          -- CASE OF MULSTICAST FIRST CELL
-- UPDATING OF MC RELATED REGISTER
          MC_TOP = S_PNT(MC_QOS)
          MC_TOP_E = 1
          MC_ADD = MC_TOP
          MC_BMAP = BMAP(MC_TOP)
-- UPDATING OF POINTER
          S_PNT(MC_QOS) = LINK(MC_TOP)
 -- UPDATING OF COUNTER
          CNT_M(MC_QOS)

   ELSE                    -- CASE OF MULTICAST SECOND CELL ONWARD
    IF INI_CNT_ < MAX      -- ACQUIRED FROM ADDRESS GENERATION COUNTER
          INI_CNT ++
          MC_ADD = INT_CNT
   ELSE                    -- ACQUIRED FROM FREE ADDRESS FIFO
    IF ADR_VAL = 1         -- WHEN FREE ADDRESS FIFO IS NOT FREE
          MC_ADD = EMP_S_PNT
          EMP_S_PNT = LINK(EMP_S_PNT)
   ELSE                    -- WHEN FREE ADDRESS FIFO IS  FREE
          STOP MC OPERATION
   ENDIF
 -- UPDATING OF COUNTER
          CNT_S(MC_QOS) ++
   ENDIF
```

```
MC_TOP_E:  MULTICAST HEAD ADDRESS IS EFFECTIVE
MC_TOP:    MULTICAST HEAD ADDRESS
MC_QOS:    QoS NUMBER OF MULTICAST CELL
MC_ADD:    MULTICAST ADDED ADDRESS
MC_BMAP:   MULTICAST REMAINING ROUTING BIT (BITMAP)
BMAP(x):   ROUTING BIT (BITMAP) OF ADDRESS x
S_PNT(x):  START POINTER OF BUFFER x
E_PNT(x):  END POINTER OF BUFFER x
EMP_S_PNT: FREE ADDRESS FIFO START POINTER
LINK(x):   ADDRESS LINKED TO ADDRESS x
CNT_M(x):  MULTICAST BUFFER QUEUE LENGTH OF QoS CLASS x
CNT_S(x):  COMMON BUFFER QUEUE LENGTH OF QoS CLASS x
INI_CNT:   INITIAL ADDRESS GENERATION COUNTER
MAX:       BUFFER LENGTH IN USE
ADR_VAL:   FREE ADDRESS IS EFFECTIVE
```

FIG.29

```
-- UPDATING OF POINTER
    LINE = TOP(MC_BMAP)
    BUF = LINE × 4 + MC_QOS
    IF CNT_L(BUF) = 0          -- PROCESS WHEN CELL BUFFER IS FREE
            S_PNT(BUF) = MC_ADD
            E_PNT(BUF) = MC_ADD
    ELSE                       -- PROCESS WHEN CELL BUFFER IS NOT FREE
            LINK(E_PNT(BUF)) = MC_ADD
            E_PNT(BUF) = MC_ADD
    ENDIF

-- UPDATING OF COUNTER
    CNT_L(BUF) ++

-- RETAINING OF BUFFER ADDRESS
    BUF_A(MC_ADD) = MC_TOP

-- UPDATING OF BITMAP
    MC_BMAP -= BITMAP(LINE)
    IF MC_BMAP = 0             -- JUDGING OF MULTICAST END
            MC_TOP_E = 0
    ENDIF
```

TOP(x): RETURN BIT NUMBER WITH 1 BEING SET FIRST AS VIEWED FROM 0 TH BIT IN BIT STRING x
LINE: DISTRIBUTION OUTGOING ROUTE NUMBER
BUF: DISTRIBUTION BUFFER NUMBER
CNT_L(x): INDIVIDUAL BUFFER QUEUE LENGTH OF QoS CLASS x
S_PNT(x): START POINTER OF BUFFER x
E_PNT(x): END POINTER OF BUFFER x
MC_ADD: MULTICAST ADDED ADDRESS
LINK(x): ADDRESS LINKED TO ADDRESS x
BUF_A(x): BUFFER ADDRESS OF ADDRESS x
MC_TOP: MULTICAST HEAD ADDRESS
MC_BMAP: MULTICAST REMAINING ROUTING BIT (BITMAP)
BITMAP(x): CONVERT CODE x INTO BITMAP
MC_TOP_E: MULTICAST HEAD ADDRESS IS EFFECTIVE

FIG.30

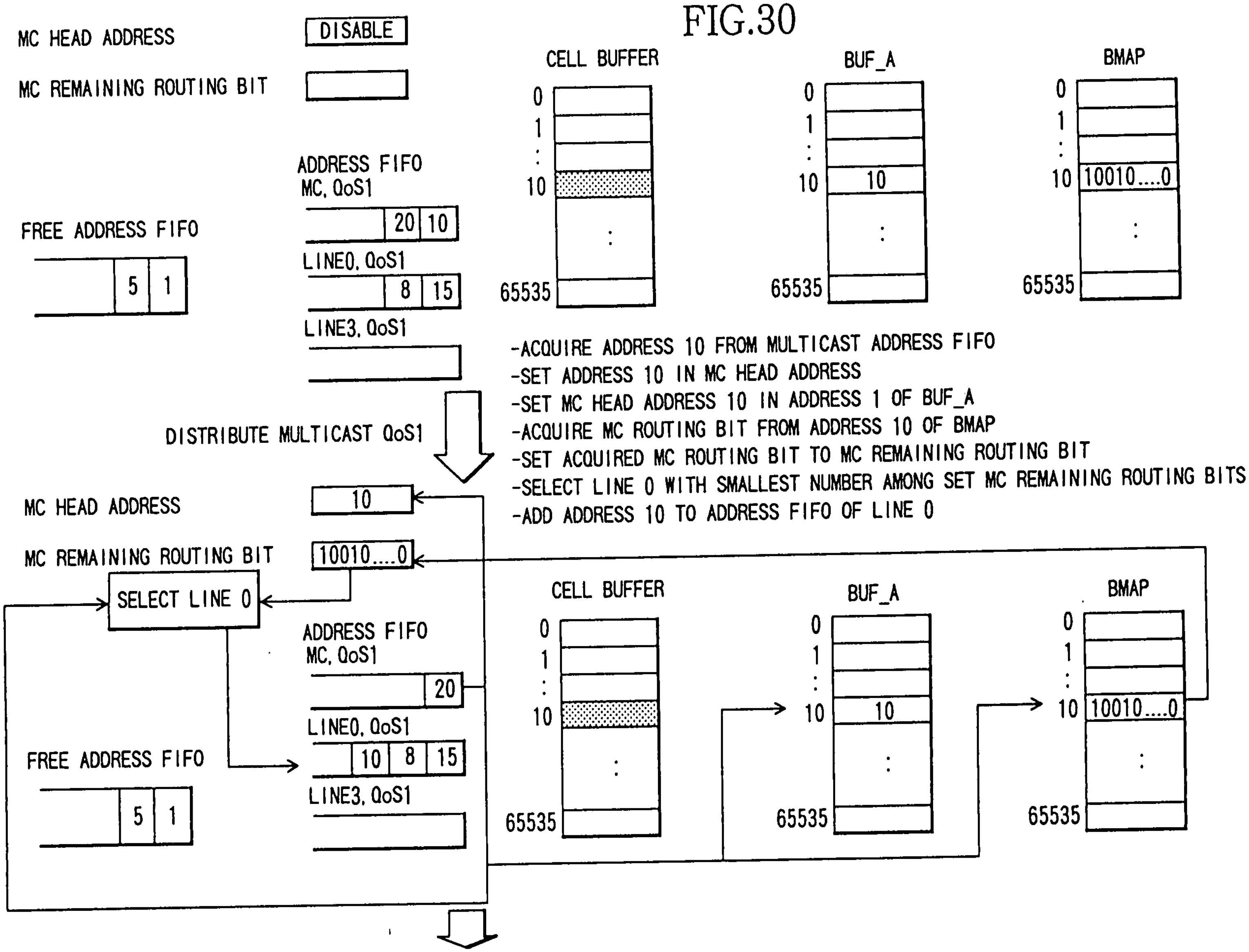

MC HEAD ADDRESS
DISABLE
MC REMAINING ROUTING BIT
FREE ADDRESS FIFO
5
1
ADDRESS FIFO
MC, QoS1
20
10
LINE0, QoS1
8
15
LINE3, QoS1
CELL BUFFER
BUF_A
BMAP
0
1
10
65535
10010....0
DISTRIBUTE MULTICAST QoS1
-ACQUIRE ADDRESS 10 FROM MULTICAST ADDRESS FIFO
-SET ADDRESS 10 IN MC HEAD ADDRESS
-SET MC HEAD ADDRESS 10 IN ADDRESS 1 OF BUF_A
-ACQUIRE MC ROUTING BIT FROM ADDRESS 10 OF BMAP
-SET ACQUIRED MC ROUTING BIT TO MC REMAINING ROUTING BIT
-SELECT LINE 0 WITH SMALLEST NUMBER AMONG SET MC REMAINING ROUTING BITS
-ADD ADDRESS 10 TO ADDRESS FIFO OF LINE 0
SELECT LINE 0

FIG.31

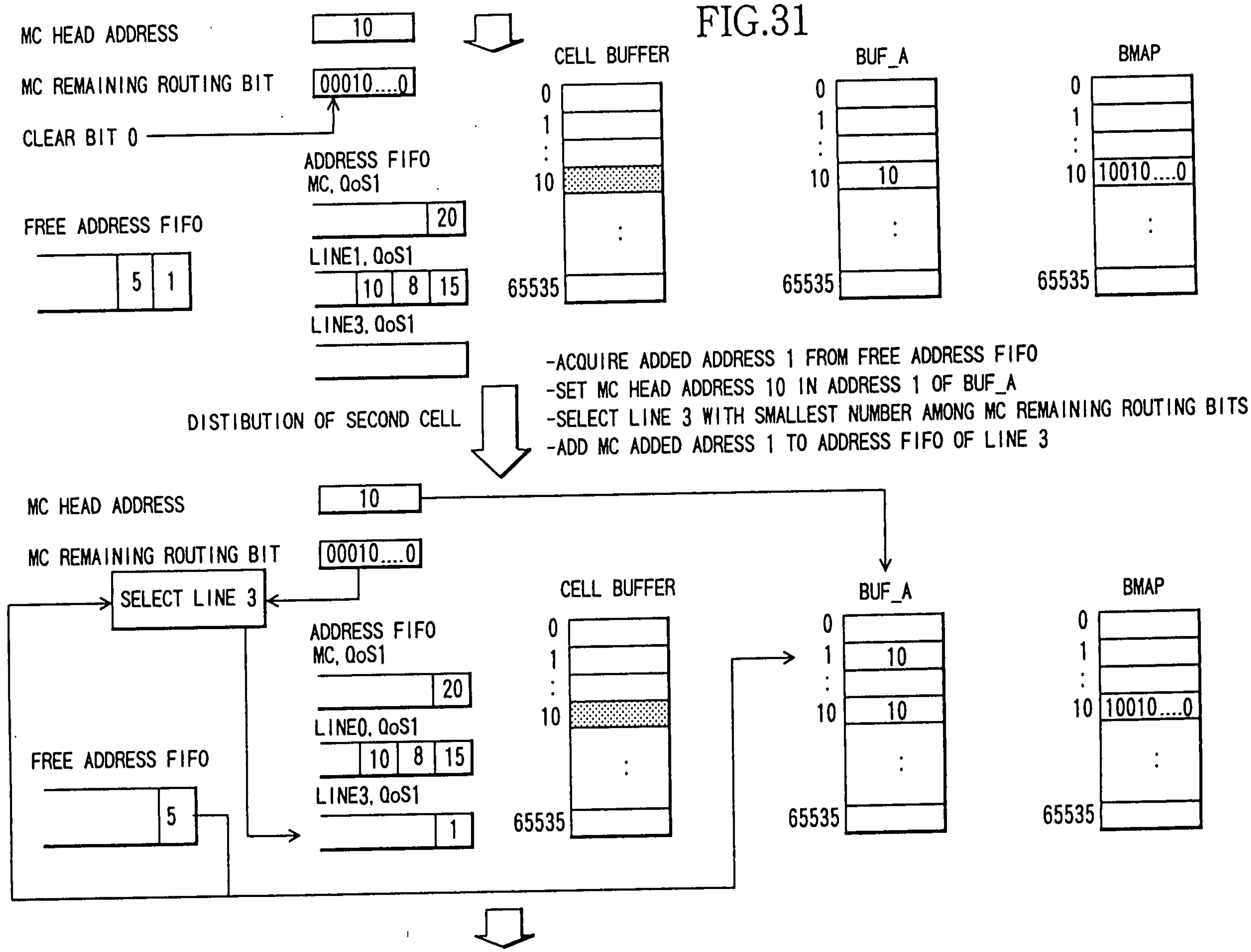

MC HEAD ADDRESS
10
MC REMAINING ROUTING BIT
00010....0
CLEAR BIT 0
FREE ADDRESS FIFO
5
1
ADDRESS FIFO
MC, QoS1
20
LINE1, QoS1
10
8
15
LINE3, QoS1
CELL BUFFER
0
1
10
65535
BUF_A
0
1
10
10
65535
BMAP
0
1
10
10010....0
65535
-ACQUIRE ADDED ADDRESS 1 FROM FREE ADDRESS FIFO
-SET MC HEAD ADDRESS 10 IN ADDRESS 1 OF BUF_A
-SELECT LINE 3 WITH SMALLEST NUMBER AMONG MC REMAINING ROUTING BITS
-ADD MC ADDED ADRESS 1 TO ADDRESS FIFO OF LINE 3
DISTIBUTION OF SECOND CELL
MC HEAD ADDRESS
10
MC REMAINING ROUTING BIT
00010....0
SELECT LINE 3
ADDRESS FIFO
MC, QoS1
20
LINE0, QoS1
10
8
15
LINE3, QoS1
1
FREE ADDRESS FIFO
5
CELL BUFFER
0
1
10
65535
BUF_A
0
1
10
10
10
65535
BMAP
0
1
10
10010....0
65535

FIG.32

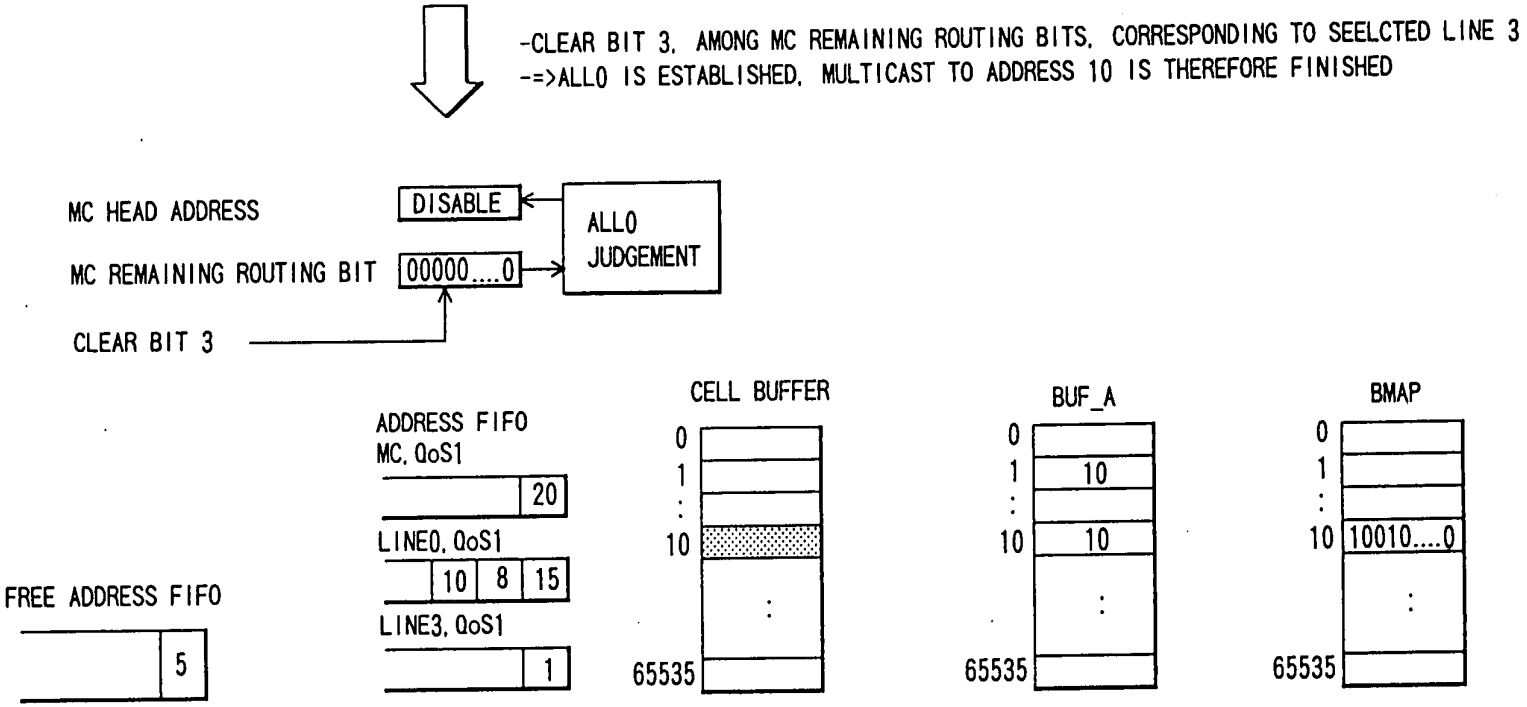

-CLEAR BIT 3, AMONG MC REMAINING ROUTING BITS, CORRESPONDING TO SEELCTED LINE 3
-=>ALL0 IS ESTABLISHED, MULTICAST TO ADDRESS 10 IS THEREFORE FINISHED
MC HEAD ADDRESS
DISABLE
ALL0 JUDGEMENT
MC REMAINING ROUTING BIT
00000....0
CLEAR BIT 3
ADDRESS FIFO MC, QoS1
20
LINE0, QoS1
10
8
15
LINE3, QoS1
1
FREE ADDRESS FIFO
5
CELL BUFFER
0
1
10
65535
BUF_A
0
1
10
10
10
65535
BMAP
0
1
10
10010....0
65535

FIG.33

```
-- ACQUISITION OF ADDRESS

   BUF = LINE × 4 + QOS
   R_ADR = S_PNT(BUF)
   BUF_ADR = BUF_A(ADR)

-- ACQUISITION OF BITMAP
   BMAP = BMAP(BUF_ADR)

-- JUDGING OF READ-OUT ADDRESS RETURN
   IF R_ADR < > BUF_ADR
            LINK(EMP_E_PNT) = R_ADR
            EMP_E_PNT = R_ADR

-- UPDATING OF COUNTER
            CNT_S(QOS)
   ENDIF

-- UPDATING OF POINTER
    S_PNT(BUF) = LINK(S_PNT(BUF))

-- UPDATING OF BITMAP
    BMAP = BITMAP(LINE)
    IF BMAP = 0          -- JUDGING OF END OF READING

-- RETURN OF BUFFER ADDRESS
           LINK(EMP_E_PNT) = BUF_ADR
           EMP_E_PNT = BUF_ADR

-- UPDATING OF COUNTER
           CNT_S(QOS)

   ENDIF

-- UPDATING OF COUNTER
   CNT_L(BUF)
```

R_ADR:	READ-OUT ADDRESS
S_PNT(x):	START POINTER OF BUFFER x
BUF:	READ-OUT BUFFER NUMBER
LINE:	READ-OUT OUTGOING ROUTE NUMBER
QoS:	READ-OUT QoS NUMBER
BUF_A(x):	BUFFER ADDRESS OF ADDRESS x
BUF_ADR:	BUFFER ADDRESS CORRESPONDING TO READ-OUT ADDRESS x
BMAP(x):	ROUTING BIT (BITMAP) OF ADDRESS x
BMAP:	ROUTING BIT (BITMAP) CORRESPONDING TO BUFFER ADDRESS
LINK(x):	ADDRESS LINKED TO ADDRESS x
EMP_E_PNT:	FREE ADDRESS FIFO END POINTER
CNT_S(x):	COMMON BUFFER QUEUE LENGTH OF QoS CLASS x
CNT_L(x):	INDIVIDUAL BUFFER QUEUE LENGTH OF QoS CLASS x
BITMAP(x):	CONVERT CODE x INTO BITMAP

FIG.34

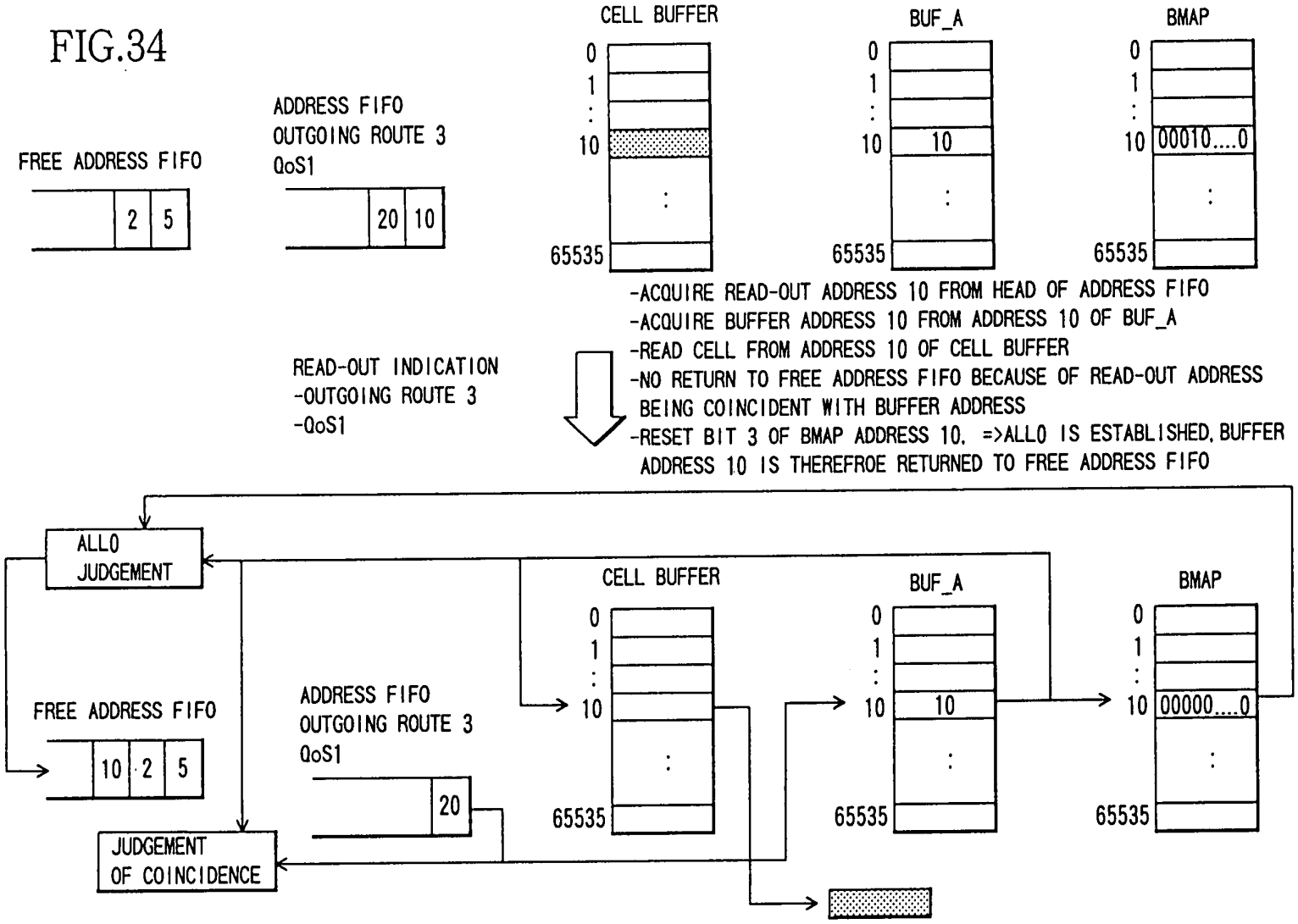

FREE ADDRESS FIFO
2
5
ADDRESS FIFO
OUTGOING ROUTE 3
QoS1
20
10
CELL BUFFER
BUF_A
BMAP
0
1
10
65535
10
00010....0
READ-OUT INDICATION
-OUTGOING ROUTE 3
-QoS1
-ACQUIRE READ-OUT ADDRESS 10 FROM HEAD OF ADDRESS FIFO
-ACQUIRE BUFFER ADDRESS 10 FROM ADDRESS 10 OF BUF_A
-READ CELL FROM ADDRESS 10 OF CELL BUFFER
-NO RETURN TO FREE ADDRESS FIFO BECAUSE OF READ-OUT ADDRESS BEING COINCIDENT WITH BUFFER ADDRESS
-RESET BIT 3 OF BMAP ADDRESS 10. =>ALL0 IS ESTABLISHED, BUFFER ADDRESS 10 IS THEREFROE RETURNED TO FREE ADDRESS FIFO
ALL0 JUDGEMENT
FREE ADDRESS FIFO
10
2
5
ADDRESS FIFO
OUTGOING ROUTE 3
QoS1
20
JUDGEMENT OF COINCIDENCE
CELL BUFFER
BUF_A
BMAP
00000....0

FIG.35

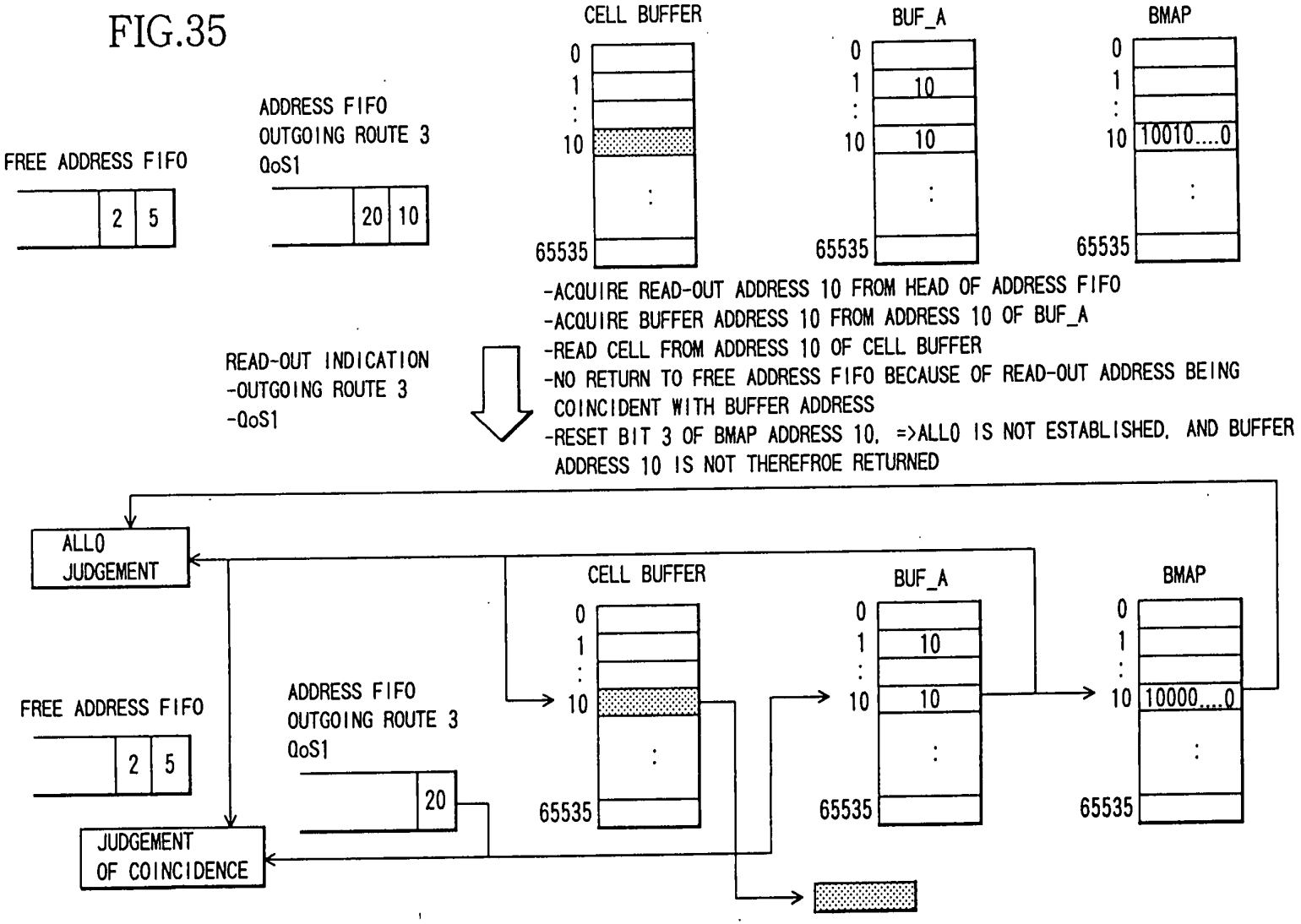
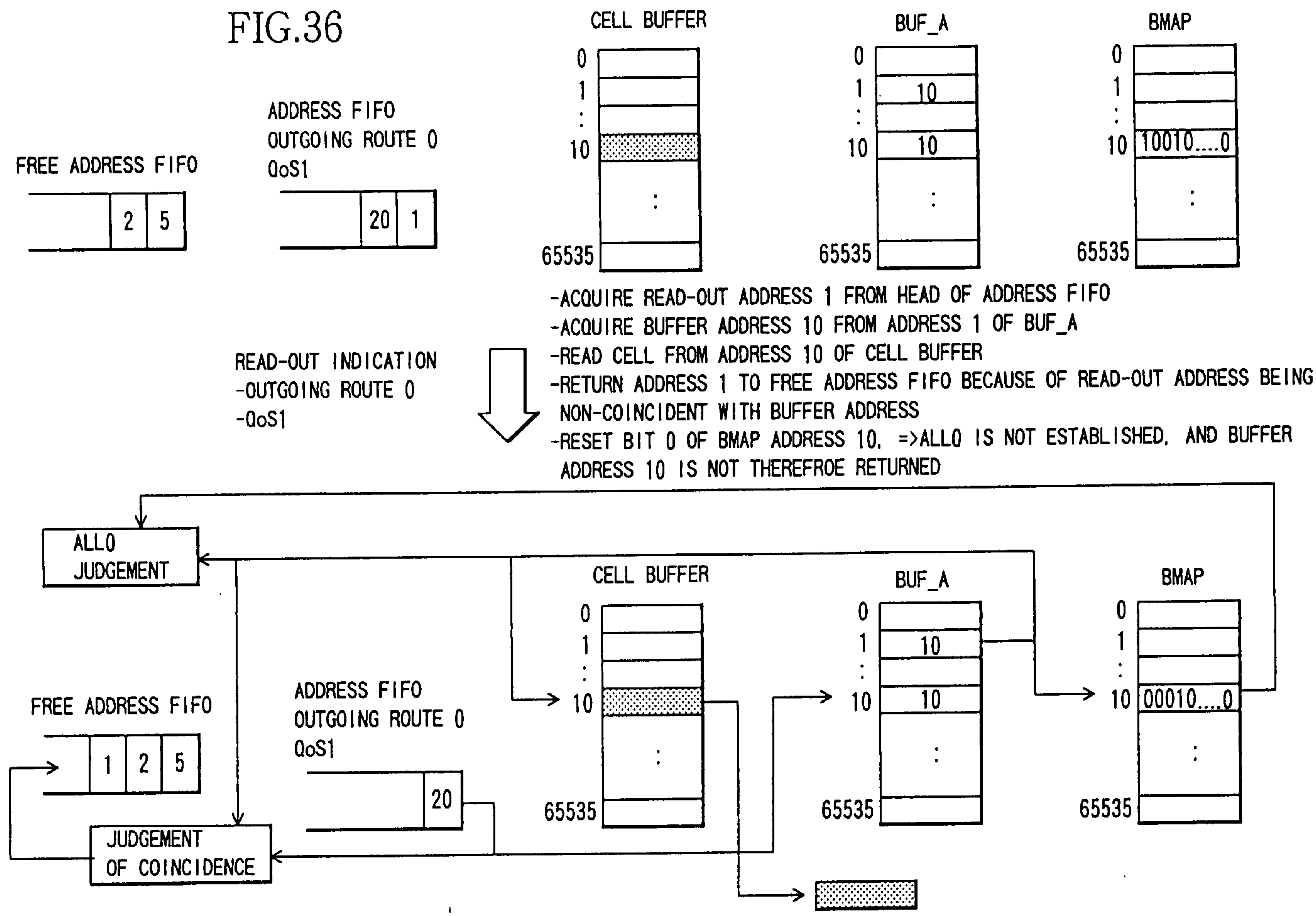

FREE ADDRESS FIFO
2
5
ADDRESS FIFO
OUTGOING ROUTE 3
QoS1
20
10
CELL BUFFER
BUF_A
BMAP
0
1
10
65535
10
10
10010....0
READ-OUT INDICATION
-OUTGOING ROUTE 3
-QoS1
-ACQUIRE READ-OUT ADDRESS 10 FROM HEAD OF ADDRESS FIFO
-ACQUIRE BUFFER ADDRESS 10 FROM ADDRESS 10 OF BUF_A
-READ CELL FROM ADDRESS 10 OF CELL BUFFER
-NO RETURN TO FREE ADDRESS FIFO BECAUSE OF READ-OUT ADDRESS BEING COINCIDENT WITH BUFFER ADDRESS
-RESET BIT 3 OF BMAP ADDRESS 10, =>ALL0 IS NOT ESTABLISHED, AND BUFFER ADDRESS 10 IS NOT THEREFROE RETURNED
ALL0
JUDGEMENT
FREE ADDRESS FIFO
2
5
ADDRESS FIFO
OUTGOING ROUTE 3
QoS1
20
JUDGEMENT
OF COINCIDENCE
CELL BUFFER
BUF_A
BMAP
10000....0

FIG.36



FREE ADDRESS FIFO
2
5
ADDRESS FIFO
OUTGOING ROUTE 0
QoS1
20
1
CELL BUFFER
BUF_A
BMAP
0
1
10
65535
10
10
10010....0
-ACQUIRE READ-OUT ADDRESS 1 FROM HEAD OF ADDRESS FIFO
-ACQUIRE BUFFER ADDRESS 10 FROM ADDRESS 1 OF BUF_A
-READ CELL FROM ADDRESS 10 OF CELL BUFFER
-RETURN ADDRESS 1 TO FREE ADDRESS FIFO BECAUSE OF READ-OUT ADDRESS BEING NON-COINCIDENT WITH BUFFER ADDRESS
-RESET BIT 0 OF BMAP ADDRESS 10. =>ALL0 IS NOT ESTABLISHED, AND BUFFER ADDRESS 10 IS NOT THEREFROE RETURNED
READ-OUT INDICATION
-OUTGOING ROUTE 0
-QoS1
ALL0
JUDGEMENT
FREE ADDRESS FIFO
1
2
5
JUDGEMENT
OF COINCIDENCE
ADDRESS FIFO
OUTGOING ROUTE 0
QoS1
20
CELL BUFFER
BUF_A
BMAP
00010....0

FIG.37

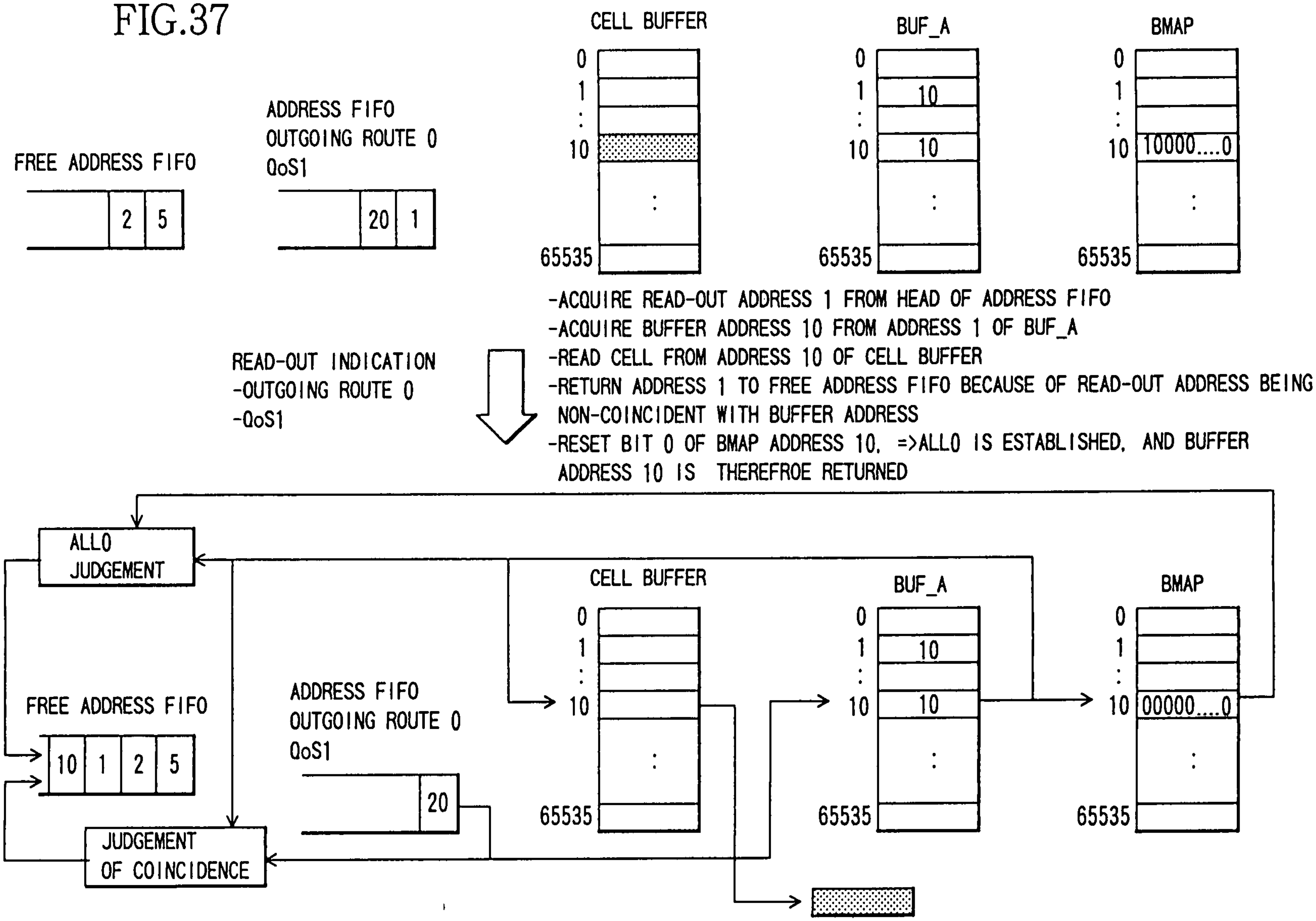

FREE ADDRESS FIFO
2 5
ADDRESS FIFO
OUTGOING ROUTE 0
QoS1
20 1
CELL BUFFER
BUF_A
BMAP
0
1
10
65535
10
10
10000....0
READ-OUT INDICATION
-OUTGOING ROUTE 0
-QoS1
-ACQUIRE READ-OUT ADDRESS 1 FROM HEAD OF ADDRESS FIFO
-ACQUIRE BUFFER ADDRESS 10 FROM ADDRESS 1 OF BUF_A
-READ CELL FROM ADDRESS 10 OF CELL BUFFER
-RETURN ADDRESS 1 TO FREE ADDRESS FIFO BECAUSE OF READ-OUT ADDRESS BEING NON-COINCIDENT WITH BUFFER ADDRESS
-RESET BIT 0 OF BMAP ADDRESS 10. =>ALL0 IS ESTABLISHED, AND BUFFER ADDRESS 10 IS THEREFROE RETURNED
ALL0
JUDGEMENT
FREE ADDRESS FIFO
10 1 2 5
JUDGEMENT
OF COINCIDENCE
ADDRESS FIFO
OUTGOING ROUTE 0
QoS1
20
CELL BUFFER
BUF_A
BMAP
00000....0

FIG.38

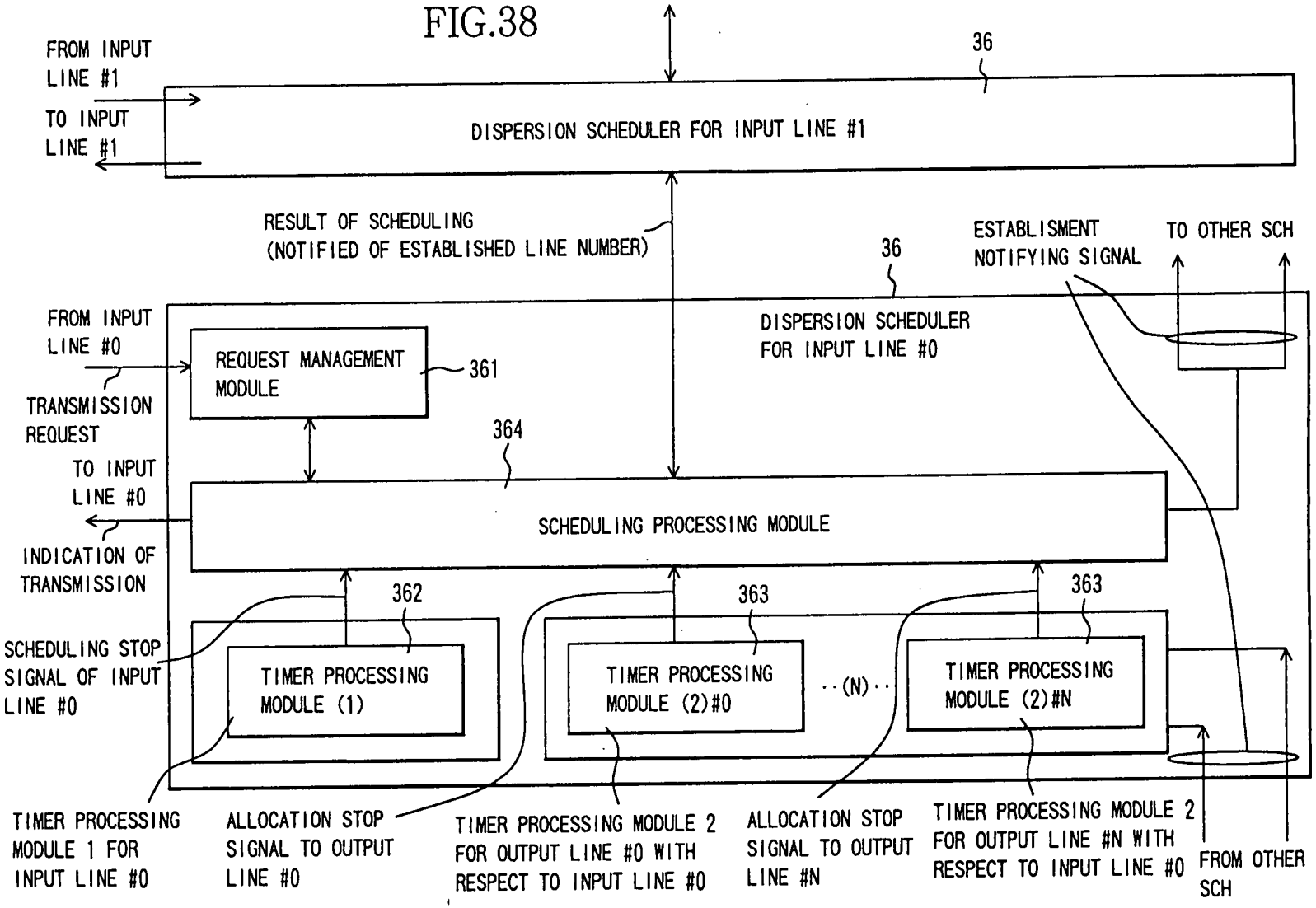

FROM INPUT LINE #1
TO INPUT LINE #1
36
DISPERSION SCHEDULER FOR INPUT LINE #1
RESULT OF SCHEDULING (NOTIFIED OF ESTABLISHED LINE NUMBER)
36
ESTABLISMENT NOTIFYING SIGNAL
TO OTHER SCH
FROM INPUT LINE #0
REQUEST MANAGEMENT MODULE
361
DISPERSION SCHEDULER FOR INPUT LINE #0
TRANSMISSION REQUEST
364
TO INPUT LINE #0
SCHEDULING PROCESSING MODULE
INDICATION OF TRANSMISSION
362
363
363
SCHEDULING STOP SIGNAL OF INPUT LINE #0
TIMER PROCESSING MODULE (1)
TIMER PROCESSING MODULE (2)#0
..(N)..
TIMER PROCESSING MODULE (2)#N
TIMER PROCESSING MODULE 1 FOR INPUT LINE #0
ALLOCATION STOP SIGNAL TO OUTPUT LINE #0
TIMER PROCESSING MODULE 2 FOR OUTPUT LINE #0 WITH RESPECT TO INPUT LINE #0
ALLOCATION STOP SIGNAL TO OUTPUT LINE #N
TIMER PROCESSING MODULE 2 FOR OUTPUT LINE #N WITH RESPECT TO INPUT LINE #0
FROM OTHER SCH

FIG.39

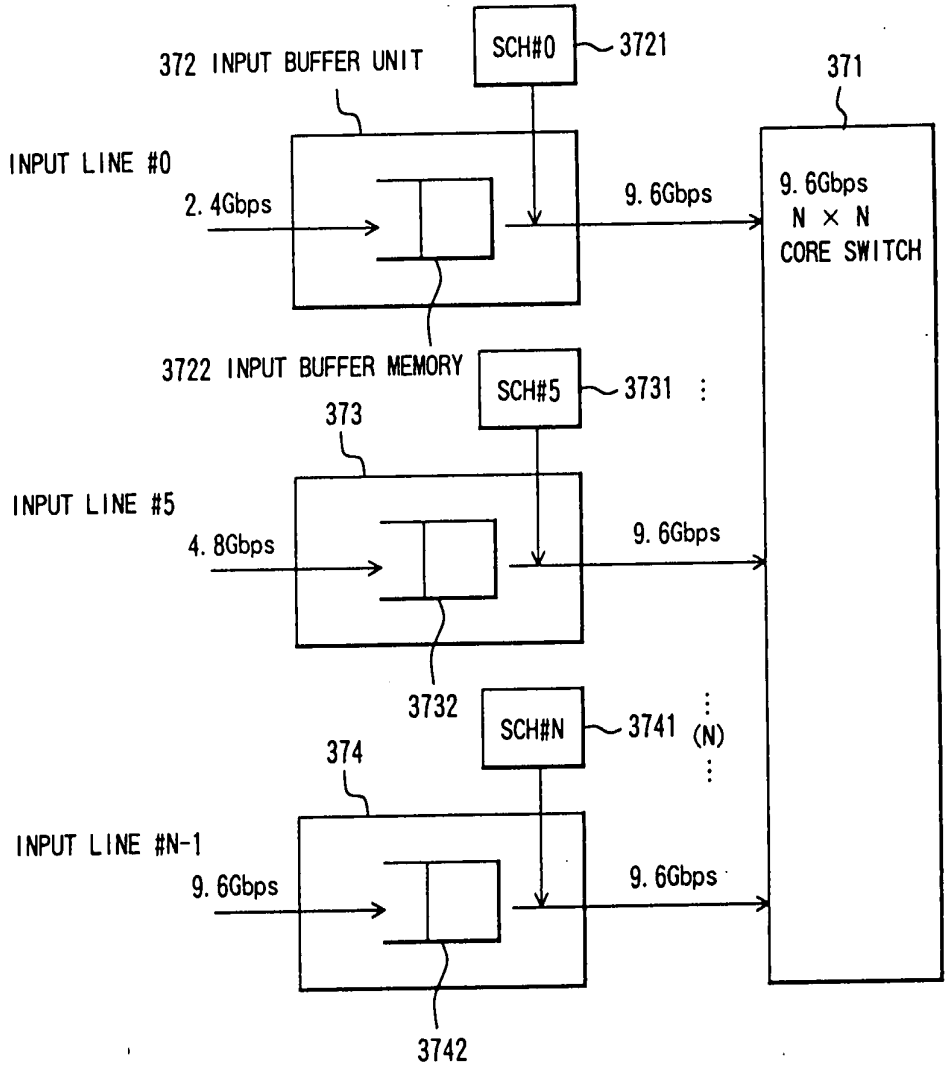

372 INPUT BUFFER UNIT
SCH#0
3721
371
INPUT LINE #0
2.4Gbps
9.6Gbps
9.6Gbps
N × N
CORE SWITCH
3722 INPUT BUFFER MEMORY
SCH#5
3731
373
INPUT LINE #5
4.8Gbps
9.6Gbps
3732
SCH#N
3741
(N)
374
INPUT LINE #N-1
9.6Gbps
9.6Gbps
3742

FIG.40

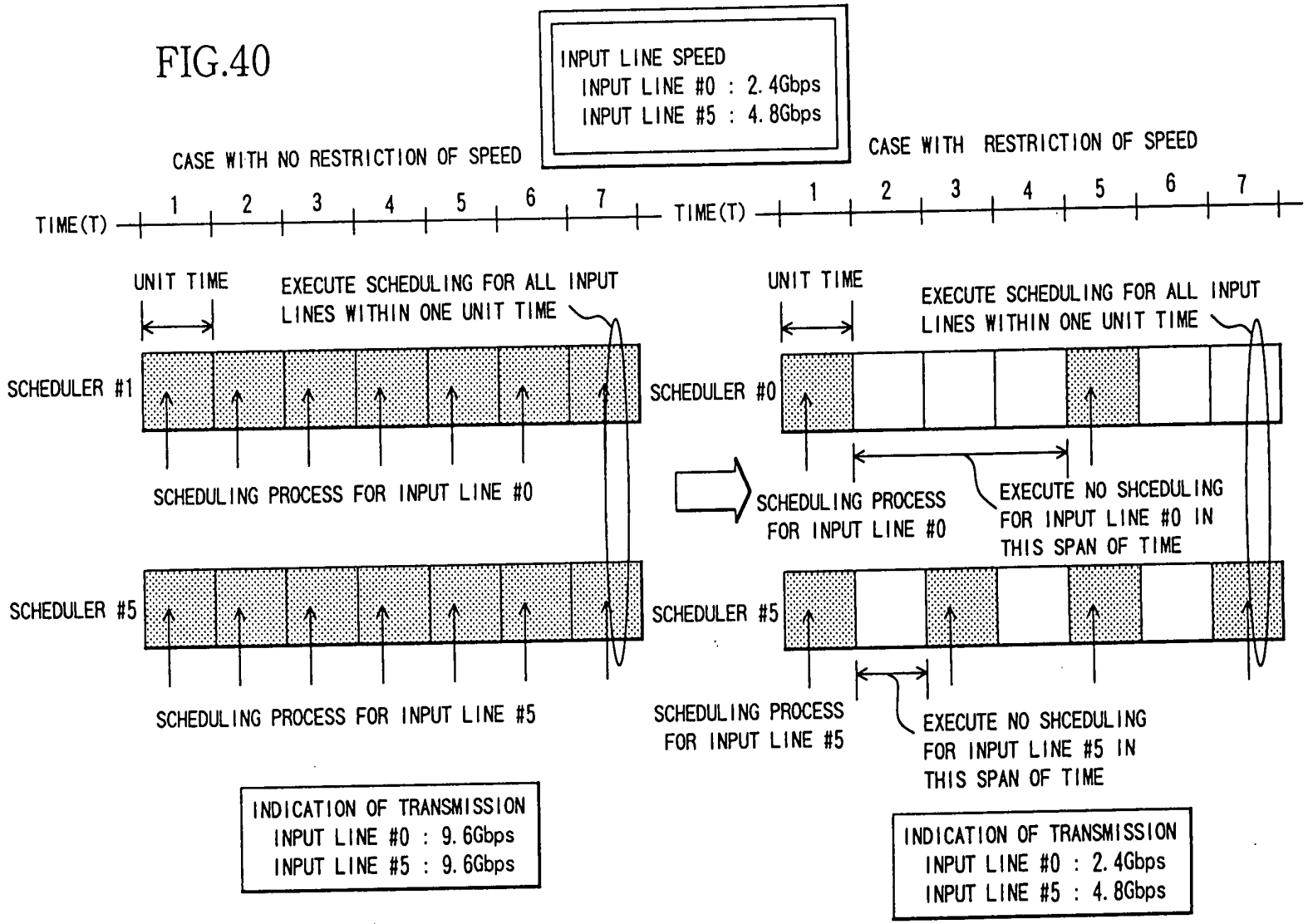

INPUT LINE SPEED
INPUT LINE #0 : 2.4Gbps
INPUT LINE #5 : 4.8Gbps
CASE WITH NO RESTRICTION OF SPEED
CASE WITH RESTRICTION OF SPEED
TIME(T)
1
2
3
4
5
6
7
UNIT TIME
EXECUTE SCHEDULING FOR ALL INPUT LINES WITHIN ONE UNIT TIME
SCHEDULER #1
SCHEDULING PROCESS FOR INPUT LINE #0
SCHEDULER #5
SCHEDULING PROCESS FOR INPUT LINE #5
INDICATION OF TRANSMISSION
INPUT LINE #0 : 9.6Gbps
INPUT LINE #5 : 9.6Gbps
SCHEDULER #0
SCHEDULING PROCESS FOR INPUT LINE #0
EXECUTE NO SHCEDULING FOR INPUT LINE #0 IN THIS SPAN OF TIME
SCHEDULER #5
SCHEDULING PROCESS FOR INPUT LINE #5
EXECUTE NO SHCEDULING FOR INPUT LINE #5 IN THIS SPAN OF TIME
INDICATION OF TRANSMISSION
INPUT LINE #0 : 2.4Gbps
INPUT LINE #5 : 4.8Gbps

FIG.41

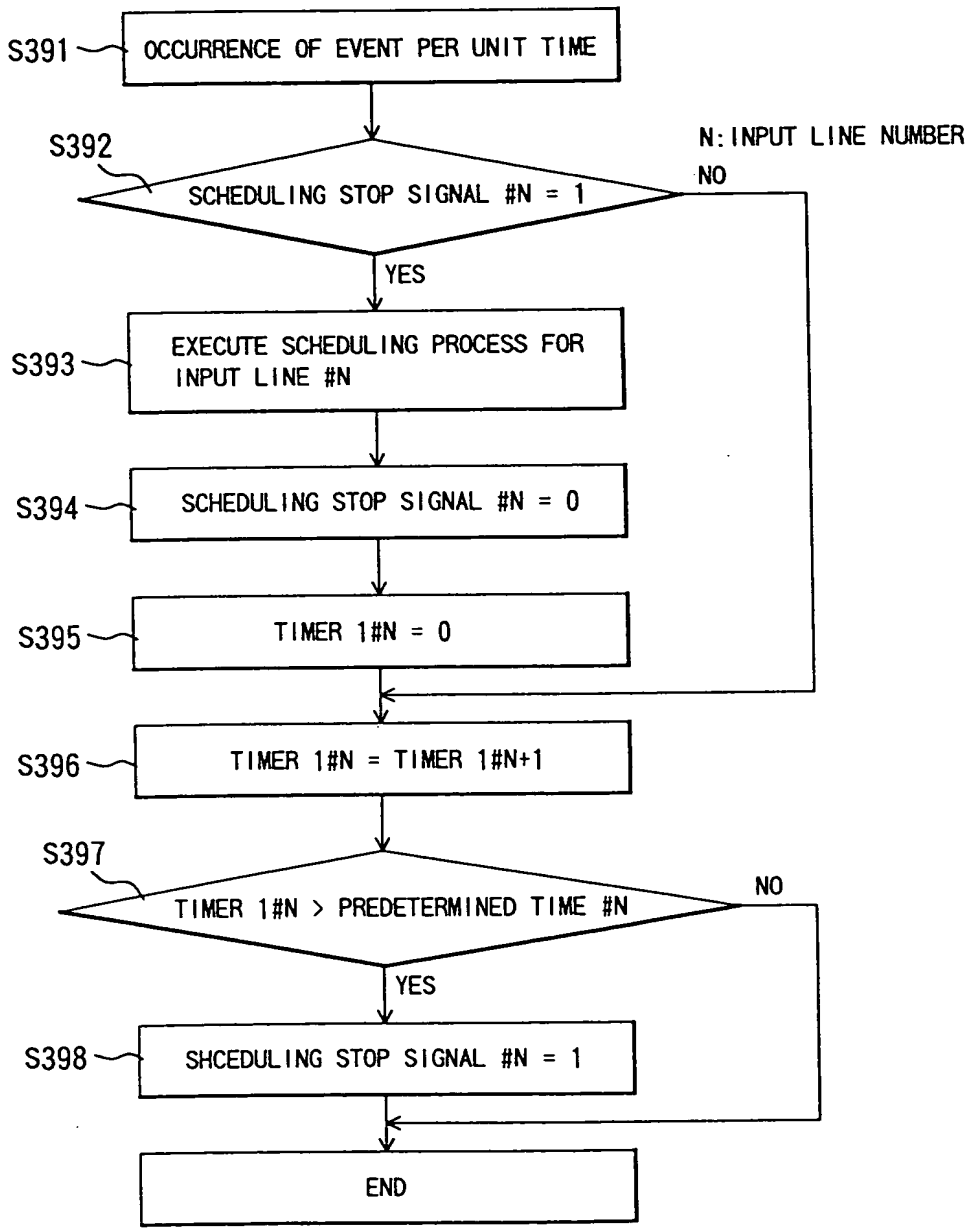

S391
OCCURRENCE OF EVENT PER UNIT TIME
S392
SCHEDULING STOP SIGNAL #N = 1
N: INPUT LINE NUMBER
NO
YES
S393
EXECUTE SCHEDULING PROCESS FOR INPUT LINE #N
S394
SCHEDULING STOP SIGNAL #N = 0
S395
TIMER 1#N = 0
S396
TIMER 1#N = TIMER 1#N+1
S397
TIMER 1#N > PREDETERMINED TIME #N
NO
YES
S398
SHCEDULING STOP SIGNAL #N = 1
END

FIG.42

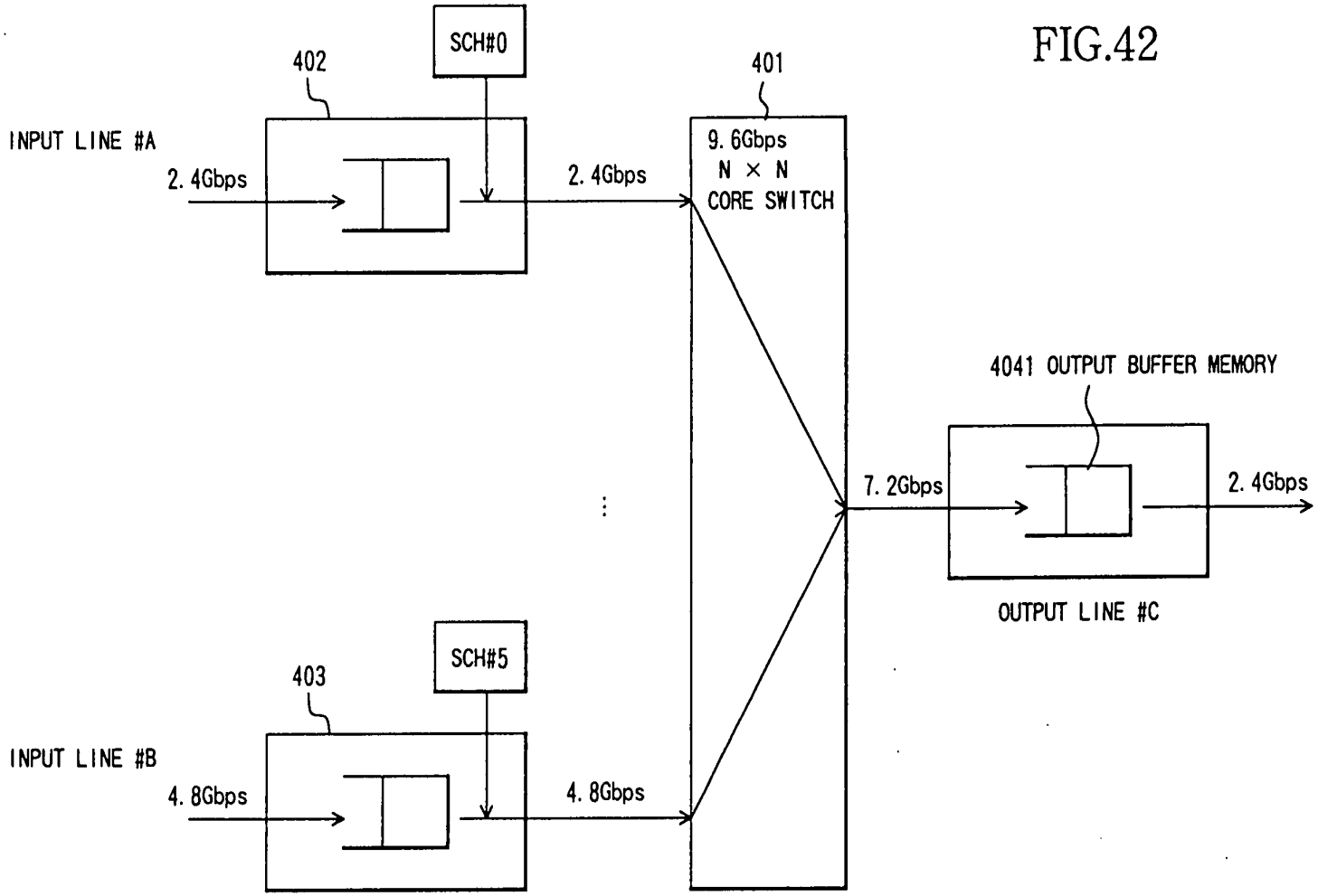

SCH#0
402
401
INPUT LINE #A
2.4Gbps
2.4Gbps
9.6Gbps
N × N
CORE SWITCH
4041 OUTPUT BUFFER MEMORY
7.2Gbps
2.4Gbps
OUTPUT LINE #C
SCH#5
403
INPUT LINE #B
4.8Gbps
4.8Gbps

FIG.43

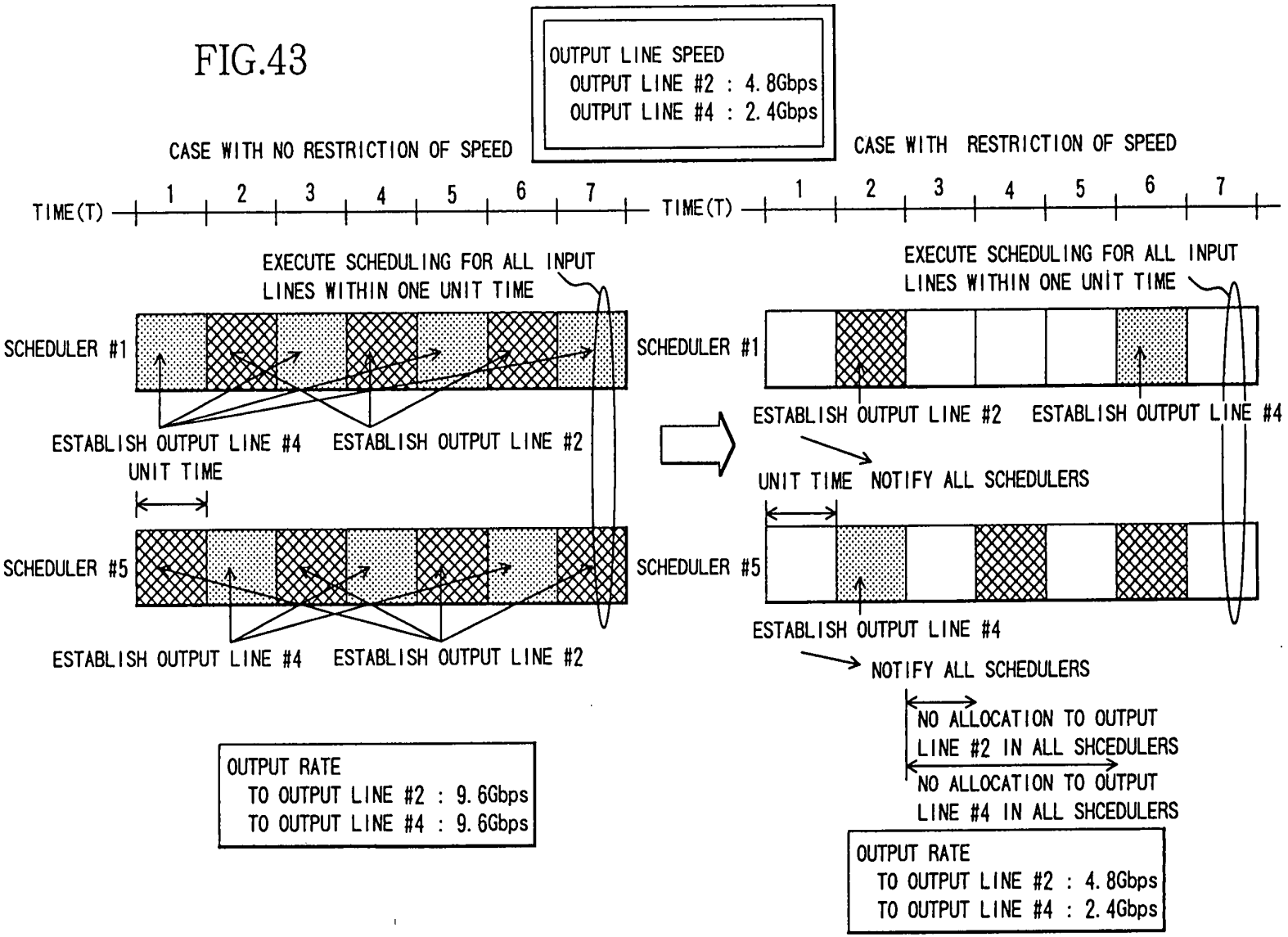

OUTPUT LINE SPEED
OUTPUT LINE #2 : 4.8Gbps
OUTPUT LINE #4 : 2.4Gbps
CASE WITH NO RESTRICTION OF SPEED
CASE WITH RESTRICTION OF SPEED
TIME(T)
1
2
3
4
5
6
7
EXECUTE SCHEDULING FOR ALL INPUT LINES WITHIN ONE UNIT TIME
SCHEDULER #1
SCHEDULER #5
ESTABLISH OUTPUT LINE #4
ESTABLISH OUTPUT LINE #2
UNIT TIME
NOTIFY ALL SCHEDULERS
NO ALLOCATION TO OUTPUT LINE #2 IN ALL SHCEDULERS
NO ALLOCATION TO OUTPUT LINE #4 IN ALL SHCEDULERS
OUTPUT RATE
TO OUTPUT LINE #2 : 9.6Gbps
TO OUTPUT LINE #4 : 9.6Gbps
OUTPUT RATE
TO OUTPUT LINE #2 : 4.8Gbps
TO OUTPUT LINE #4 : 2.4Gbps

FIG.44

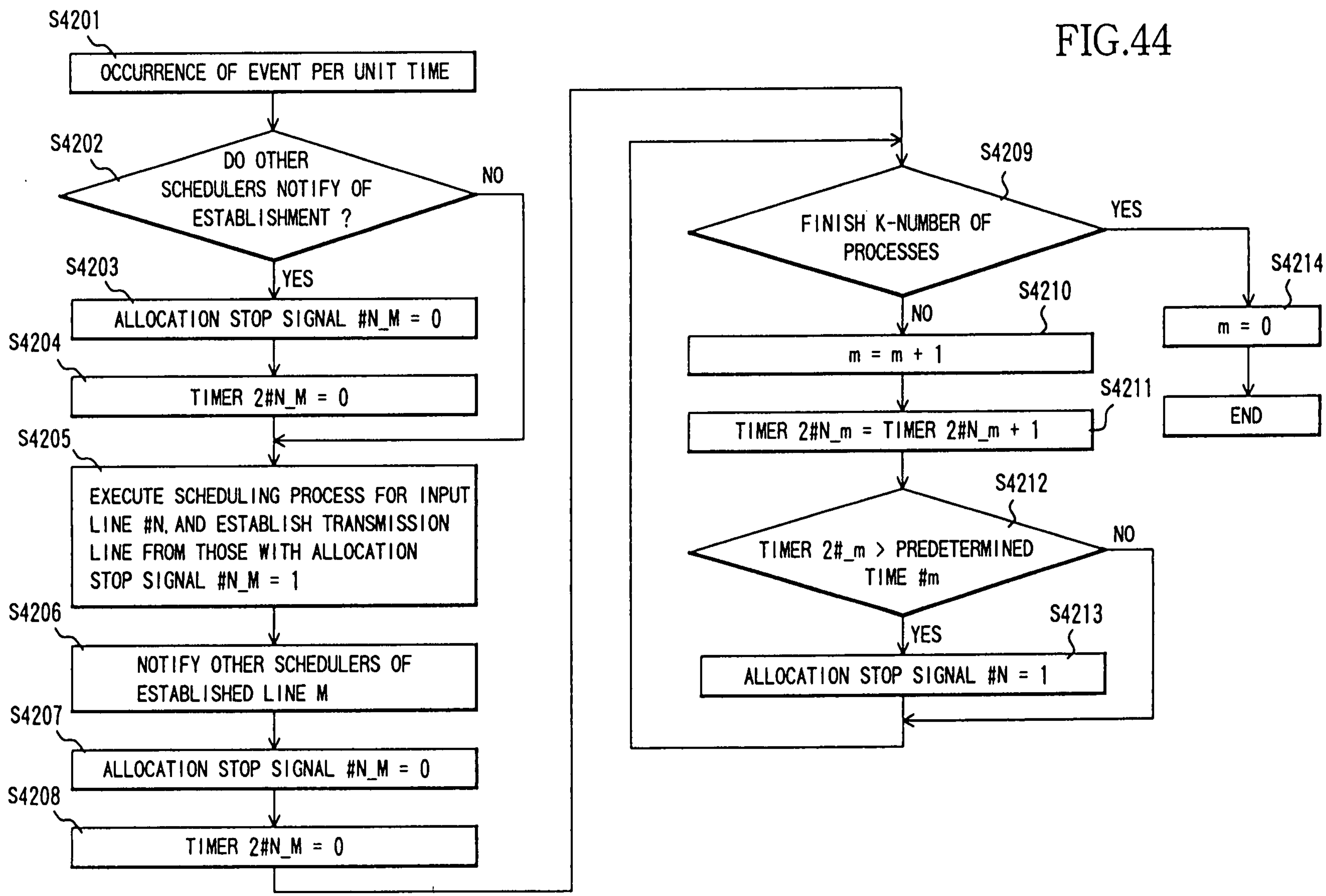

S4201
OCCURRENCE OF EVENT PER UNIT TIME
S4202
DO OTHER SCHEDULERS NOTIFY OF ESTABLISHMENT ?
NO
YES
S4203
ALLOCATION STOP SIGNAL #N_M = 0
S4204
TIMER 2#N_M = 0
S4205
EXECUTE SCHEDULING PROCESS FOR INPUT LINE #N, AND ESTABLISH TRANSMISSION LINE FROM THOSE WITH ALLOCATION STOP SIGNAL #N_M = 1
S4206
NOTIFY OTHER SCHEDULERS OF ESTABLISHED LINE M
S4207
ALLOCATION STOP SIGNAL #N_M = 0
S4208
TIMER 2#N_M = 0
S4209
FINISH K-NUMBER OF PROCESSES
YES
NO
S4210
m = m + 1
S4211
TIMER 2#N_m = TIMER 2#N_m + 1
S4212
TIMER 2#_m > PREDETERMINED TIME #m
NO
YES
S4213
ALLOCATION STOP SIGNAL #N = 1
S4214
m = 0
END

FIG.45

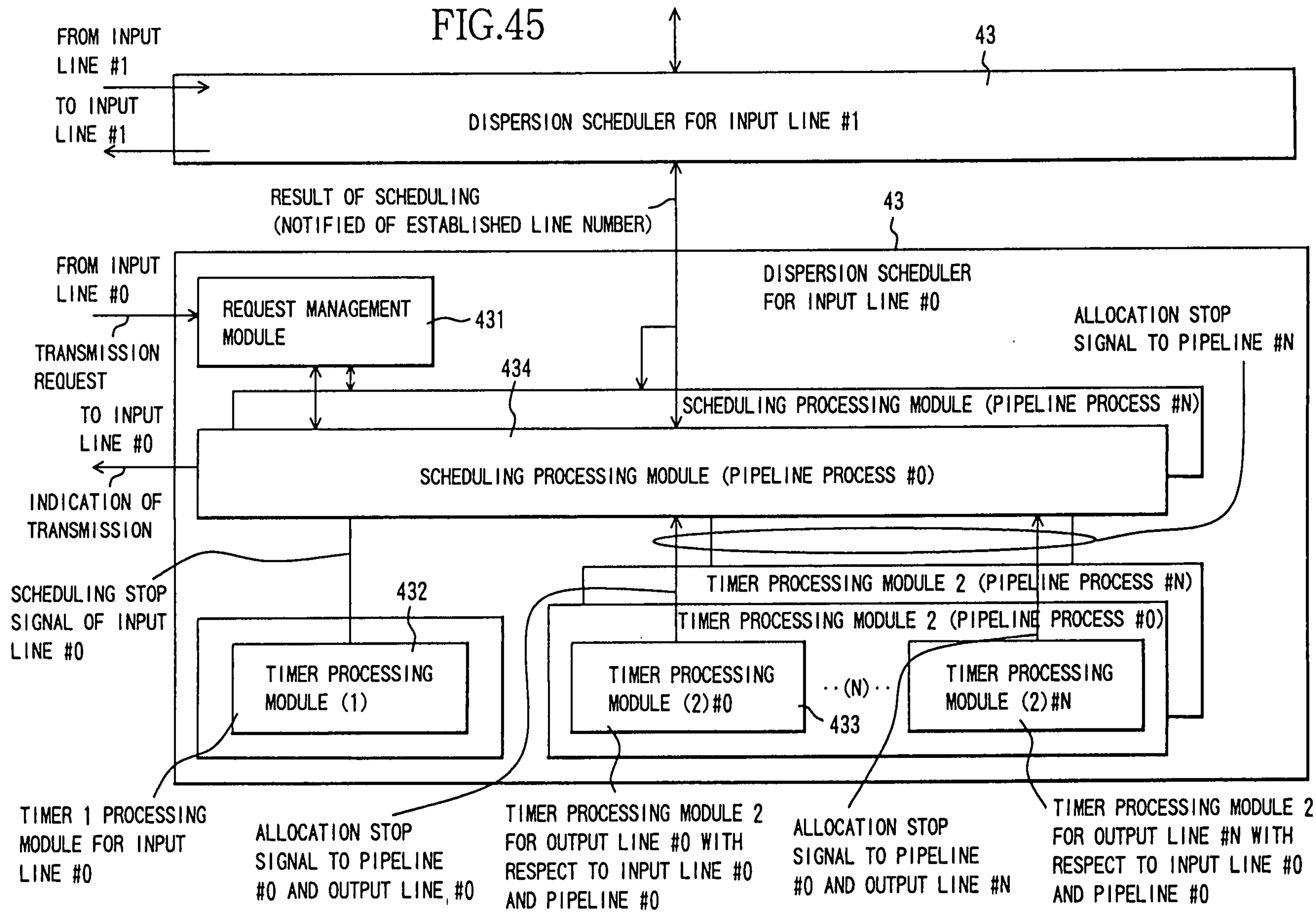
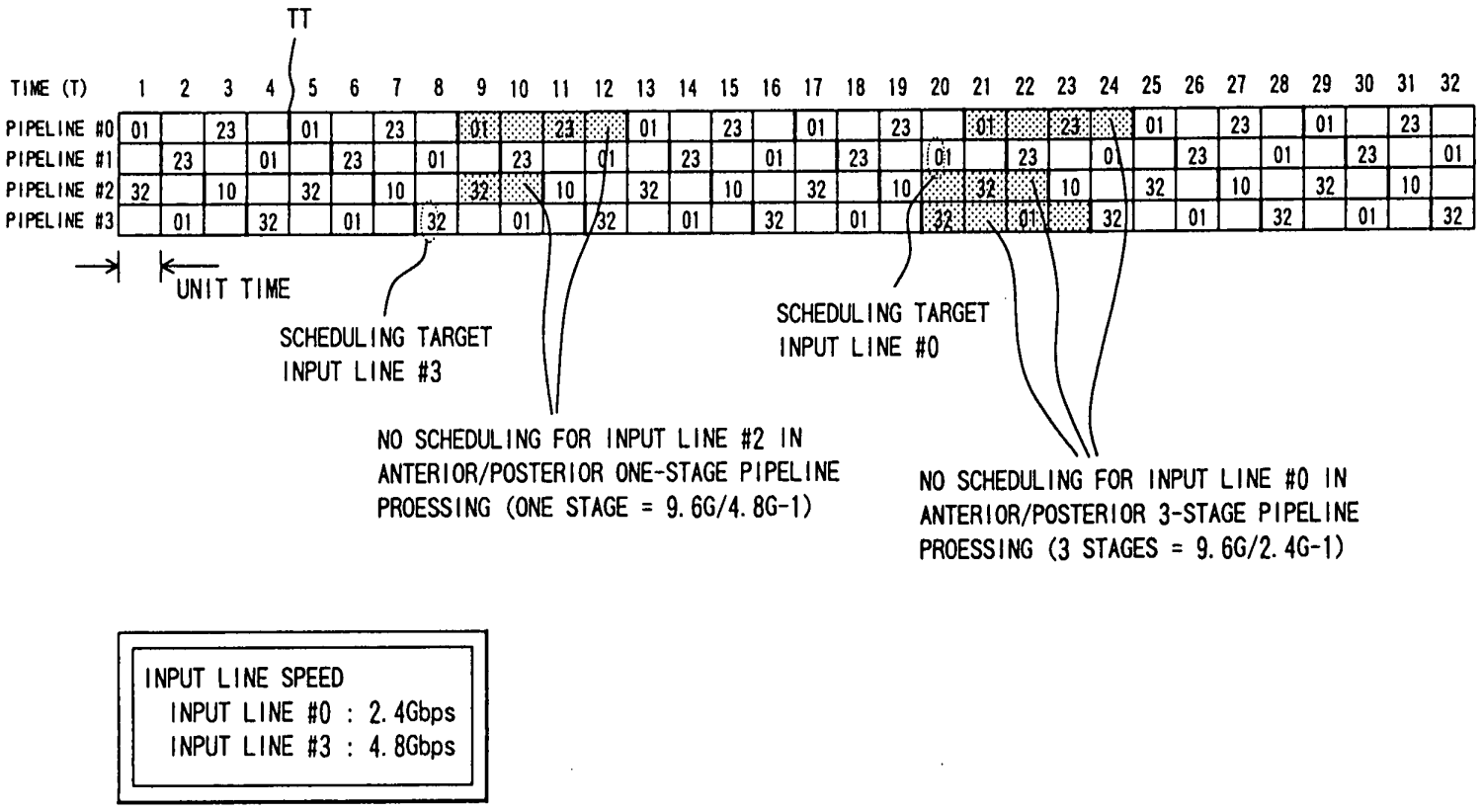

FROM INPUT LINE #1
TO INPUT LINE #1
DISPERSION SCHEDULER FOR INPUT LINE #1
43
RESULT OF SCHEDULING
(NOTIFIED OF ESTABLISHED LINE NUMBER)
43
FROM INPUT LINE #0
TRANSMISSION REQUEST
REQUEST MANAGEMENT MODULE
431
DISPERSION SCHEDULER FOR INPUT LINE #0
ALLOCATION STOP SIGNAL TO PIPELINE #N
434
TO INPUT LINE #0
SCHEDULING PROCESSING MODULE (PIPELINE PROCESS #N)
SCHEDULING PROCESSING MODULE (PIPELINE PROCESS #0)
INDICATION OF TRANSMISSION
SCHEDULING STOP SIGNAL OF INPUT LINE #0
432
TIMER PROCESSING MODULE (1)
TIMER PROCESSING MODULE 2 (PIPELINE PROCESS #N)
TIMER PROCESSING MODULE 2 (PIPELINE PROCESS #0)
TIMER PROCESSING MODULE (2)#0
··(N)··
433
TIMER PROCESSING MODULE (2)#N
TIMER 1 PROCESSING MODULE FOR INPUT LINE #0
ALLOCATION STOP SIGNAL TO PIPELINE #0 AND OUTPUT LINE #0
TIMER PROCESSING MODULE 2 FOR OUTPUT LINE #0 WITH RESPECT TO INPUT LINE #0 AND PIPELINE #0
ALLOCATION STOP SIGNAL TO PIPELINE #0 AND OUTPUT LINE #N
TIMER PROCESSING MODULE 2 FOR OUTPUT LINE #N WITH RESPECT TO INPUT LINE #0 AND PIPELINE #0

FIG.46



INPUT LINE SPEED
INPUT LINE #0 : 2.4Gbps
INPUT LINE #3 : 4.8Gbps

FIG.47

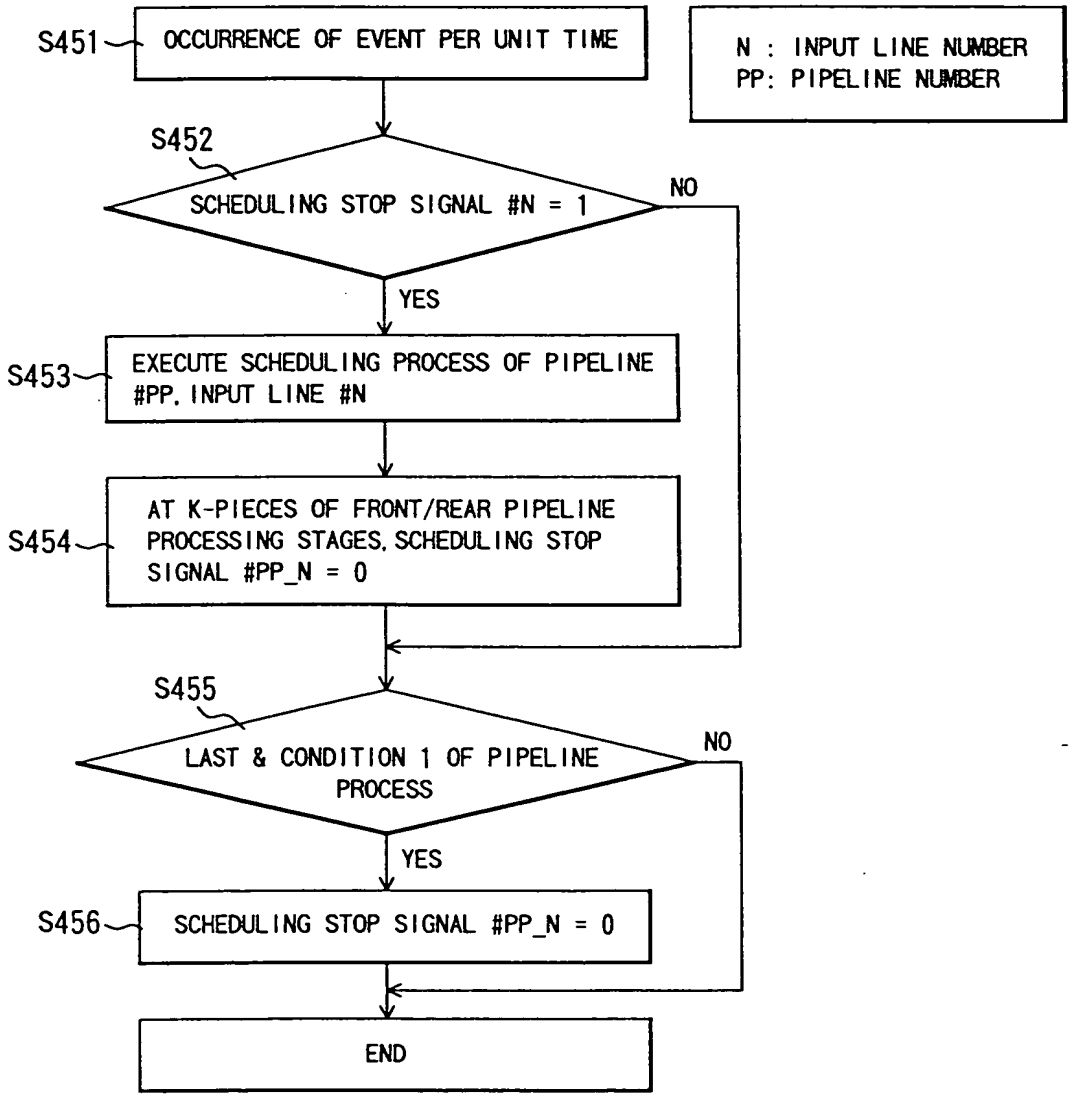

S451
OCCURRENCE OF EVENT PER UNIT TIME
N : INPUT LINE NUMBER
PP: PIPELINE NUMBER
S452
SCHEDULING STOP SIGNAL #N = 1
NO
YES
S453
EXECUTE SCHEDULING PROCESS OF PIPELINE #PP, INPUT LINE #N
S454
AT K-PIECES OF FRONT/REAR PIPELINE PROCESSING STAGES, SCHEDULING STOP SIGNAL #PP_N = 0
S455
LAST & CONDITION 1 OF PIPELINE PROCESS
NO
YES
S456
SCHEDULING STOP SIGNAL #PP_N = 0
END

FIG.48

TIME (T)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIPELINE #0	01		23		01		23		01		23		01		23	
PIPELINE #1		23		01		23		01		23		01		23		01
PIPELINE #2	32		10		32		10		32		10		32		10	
PIPELINE #3		01		32		01		32		01		32		01		32

TIME (T)	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIPELINE #0	01		23		01		23		01		23		01		23	
PIPELINE #1		23		01		23		01		23		01		23		01
PIPELINE #2	32		10		32		10		32		10		32		10	
PIPELINE #3		01		32		01		32		01		32		01		32

UNIT TIME

ESTABLISH OUTPUT LINE #3 WITH RESPECT TO INPUT LINE #0

NO ALLOCATION TO OUTPUT LINE #3 IN THIS SPAN OF TIME IN PIPELINE #0

ESTABLISH OUTPUT LINE #0 WITH RESPECT TO INPUT LINE #2

ESTABLISH OUTPUT LINE #3 WITH RESPECT TO INPUT LINE #1

NO ALLOCATION TO OUTPUT LINE #0 IN THIS SPAN OF TIME IN PIPELINE #3

NO ALLOCATION TO OUTPUT LINE #3 IN THIS SPAN OF TIME IN PIPELINE #3

OUTPUT LINE SPEED
OUTPUT LINE #0 : 2.4Gbps
OUTPUT LINE #3 : 4.8Gbps

FIG.49

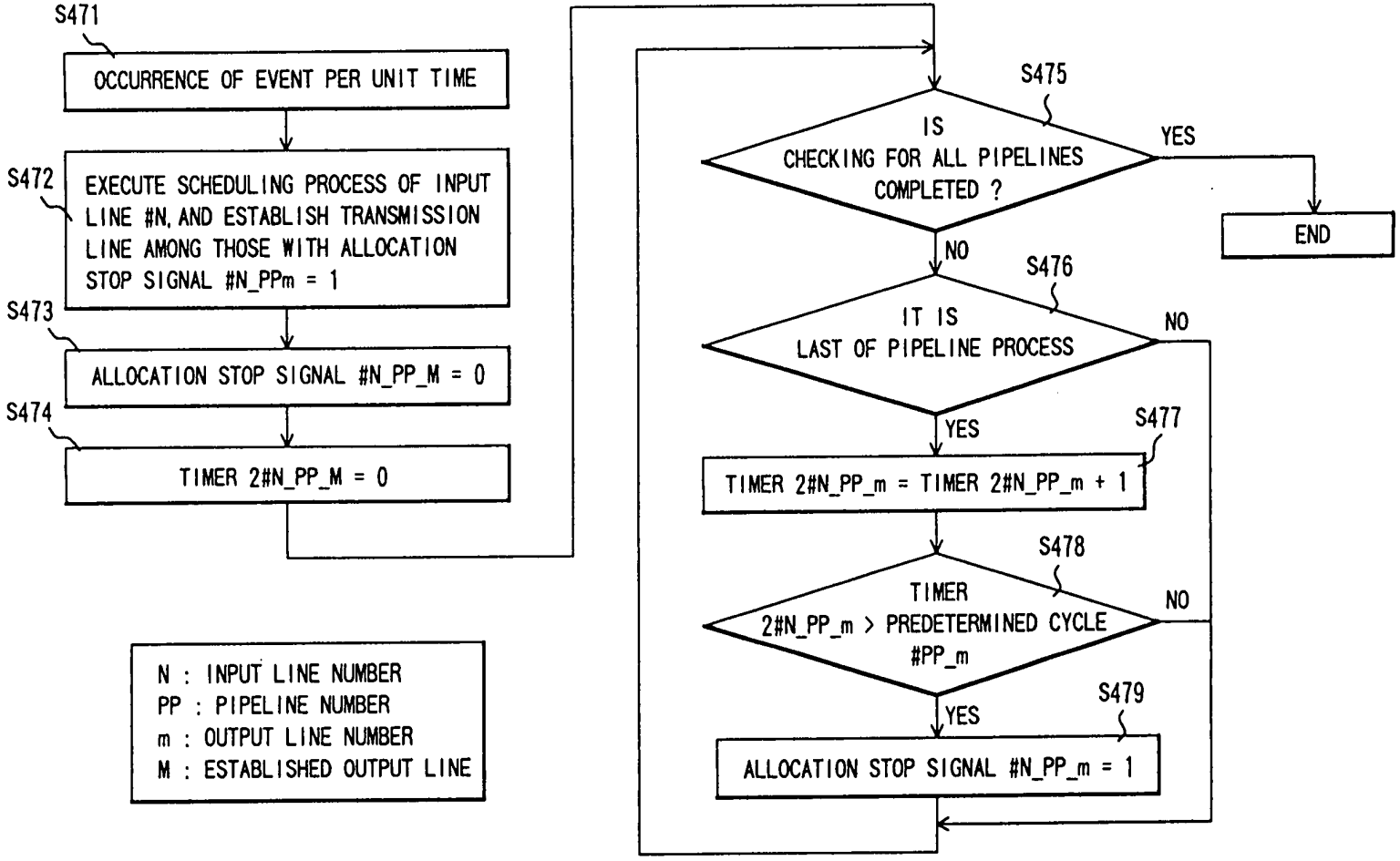

S471
OCCURRENCE OF EVENT PER UNIT TIME
S472
EXECUTE SCHEDULING PROCESS OF INPUT LINE #N, AND ESTABLISH TRANSMISSION LINE AMONG THOSE WITH ALLOCATION STOP SIGNAL #N_PPm = 1
S473
ALLOCATION STOP SIGNAL #N_PP_M = 0
S474
TIMER 2#N_PP_M = 0
S475
IS CHECKING FOR ALL PIPELINES COMPLETED ?
YES
END
NO
S476
IT IS LAST OF PIPELINE PROCESS
NO
YES
S477
TIMER 2#N_PP_m = TIMER 2#N_PP_m + 1
S478
TIMER 2#N_PP_m > PREDETERMINED CYCLE #PP_m
NO
YES
S479
ALLOCATION STOP SIGNAL #N_PP_m = 1
N : INPUT LINE NUMBER
PP : PIPELINE NUMBER
m : OUTPUT LINE NUMBER
M : ESTABLISHED OUTPUT LINE

FIG.50

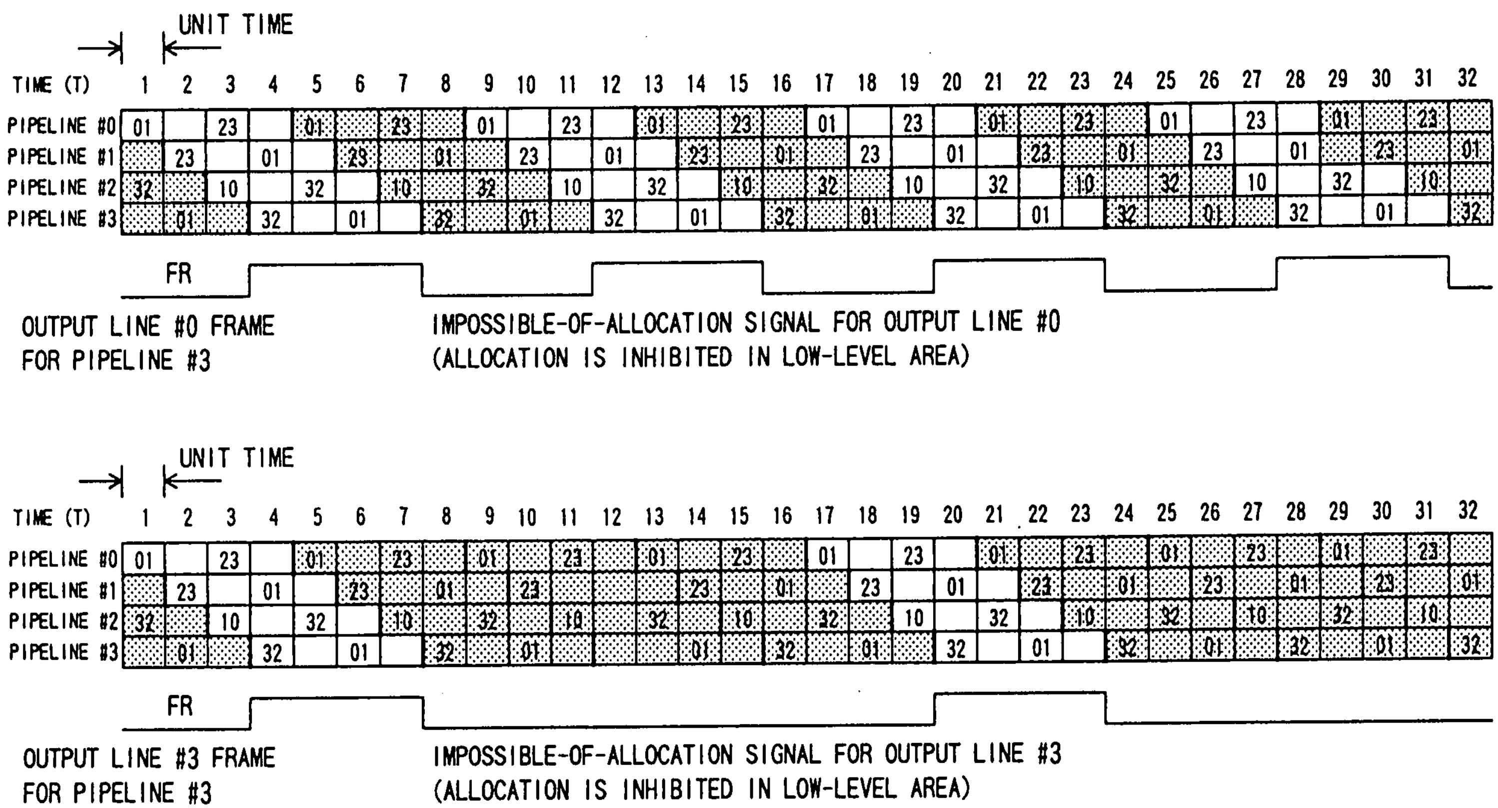

UNIT TIME
TIME (T)
PIPELINE #0
PIPELINE #1
PIPELINE #2
PIPELINE #3
FR
OUTPUT LINE #0 FRAME
FOR PIPELINE #3
IMPOSSIBLE-OF-ALLOCATION SIGNAL FOR OUTPUT LINE #0
(ALLOCATION IS INHIBITED IN LOW-LEVEL AREA)
UNIT TIME
TIME (T)
PIPELINE #0
PIPELINE #1
PIPELINE #2
PIPELINE #3
FR
OUTPUT LINE #3 FRAME
FOR PIPELINE #3
IMPOSSIBLE-OF-ALLOCATION SIGNAL FOR OUTPUT LINE #3
(ALLOCATION IS INHIBITED IN LOW-LEVEL AREA)

FIG.51

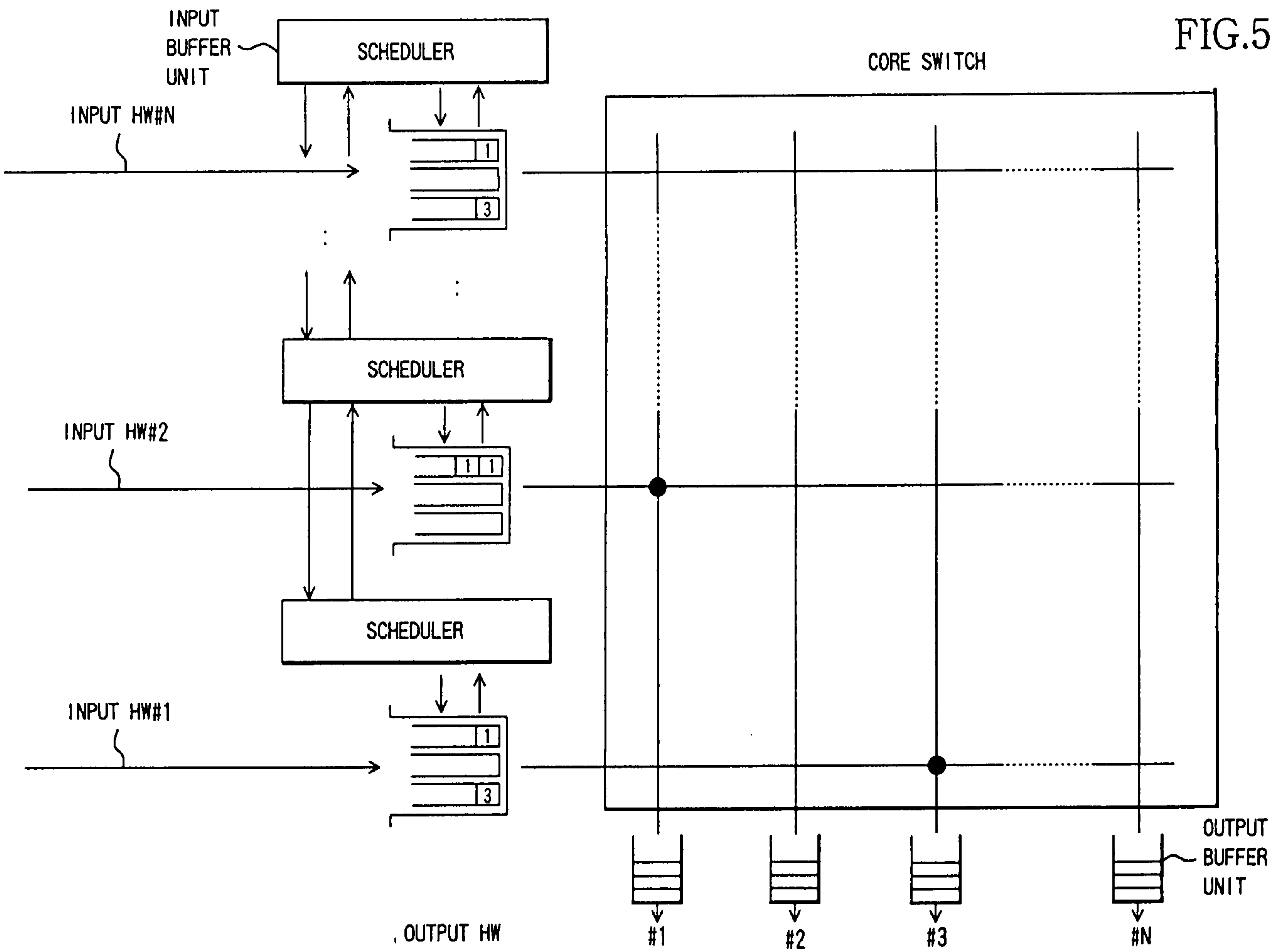

INPUT
BUFFER
UNIT
SCHEDULER
INPUT HW#N
1
3
CORE SWITCH
SCHEDULER
INPUT HW#2
1
1
SCHEDULER
INPUT HW#1
1
3
OUTPUT
BUFFER
UNIT
OUTPUT HW
#1
#2
#3
#N

FIG.1

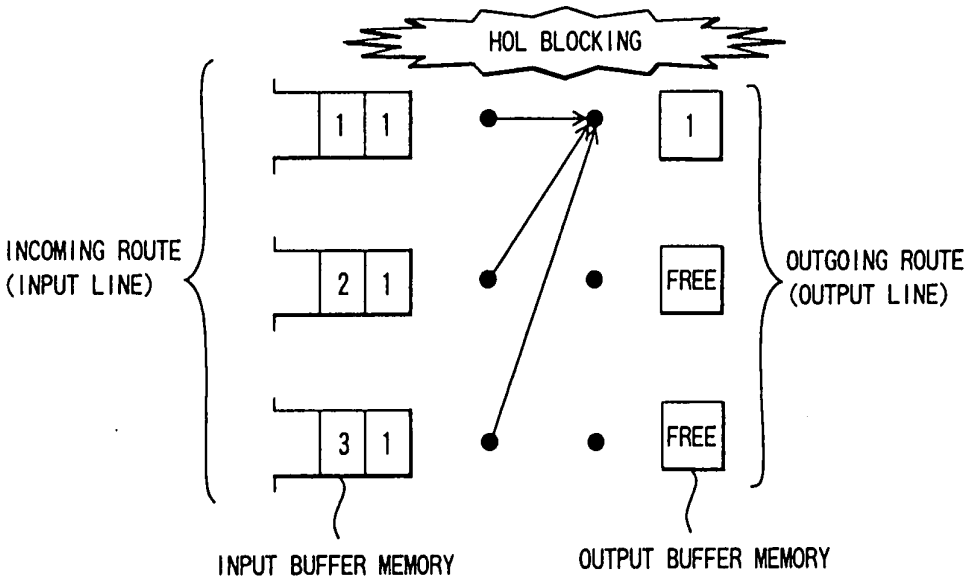

HOL BLOCKING
INCOMING ROUTE
(INPUT LINE)
1 1
2 1
3 1
1
FREE
FREE
OUTGOING ROUTE
(OUTPUT LINE)
INPUT BUFFER MEMORY
OUTPUT BUFFER MEMORY

FIG.2

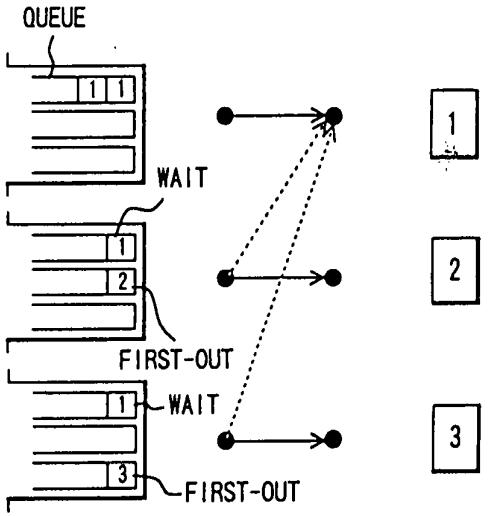

QUEUE
1 1
WAIT
1
2
FIRST-OUT
1
WAIT
3
FIRST-OUT
1
2
3

FIG.3

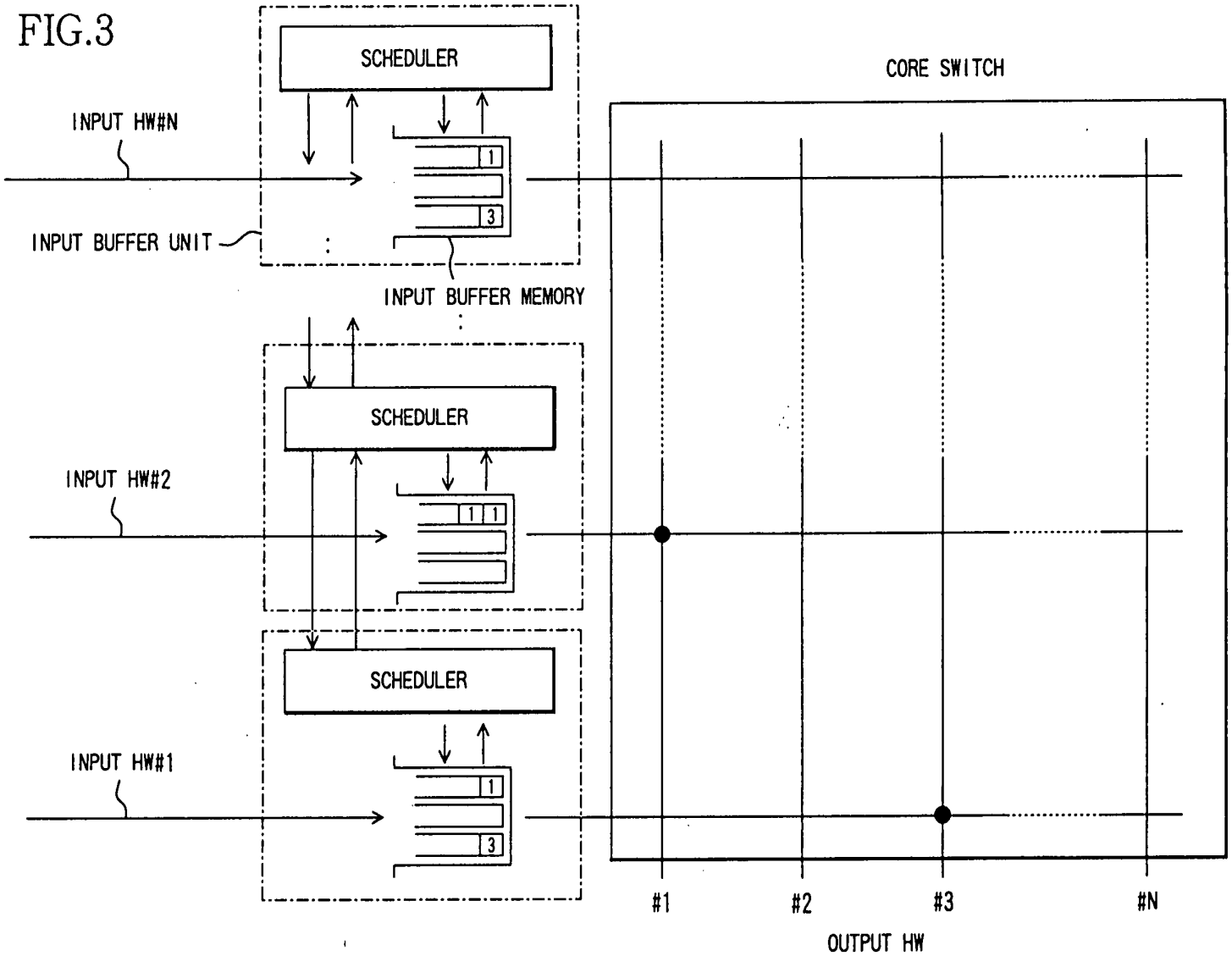
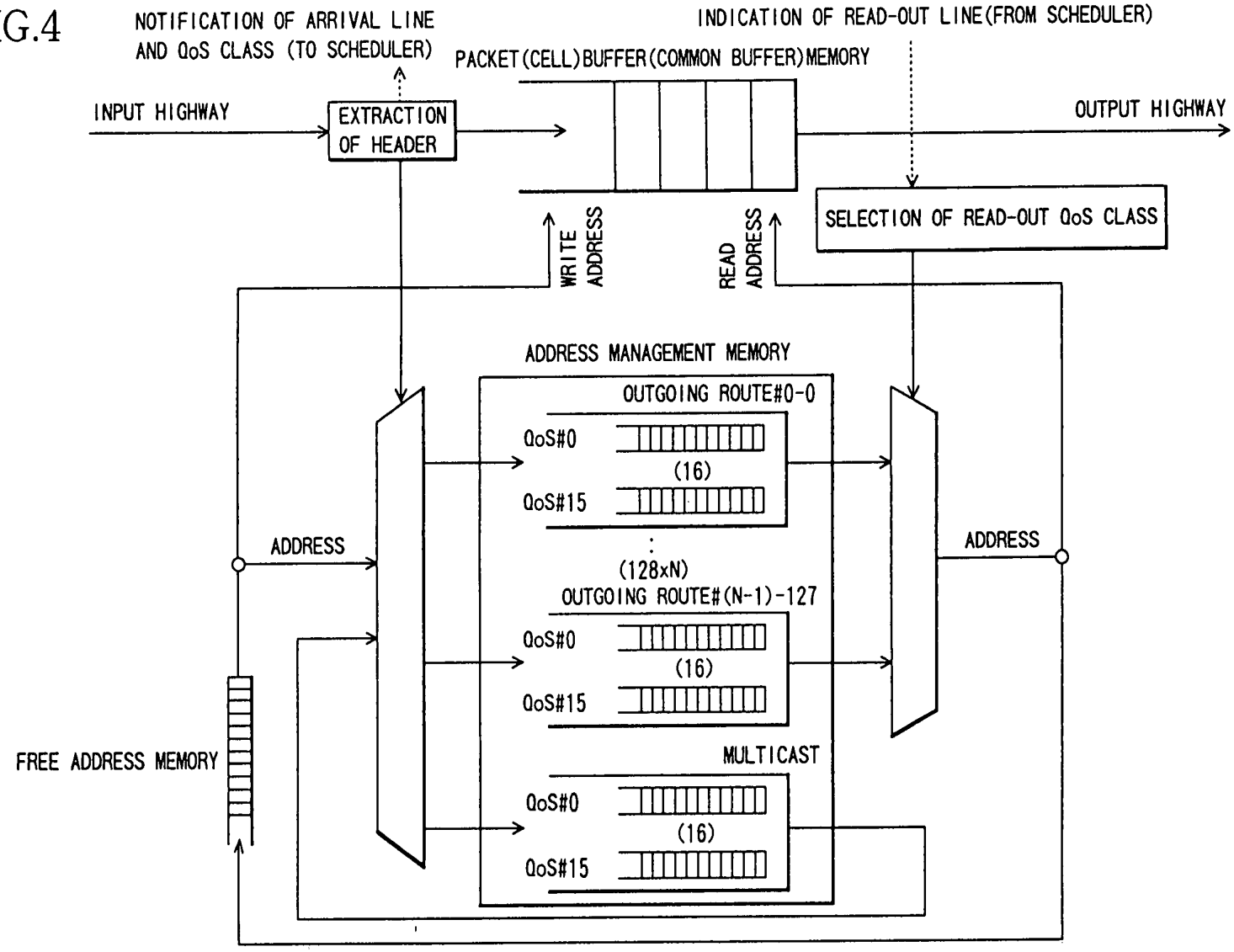

SCHEDULER
CORE SWITCH
INPUT HW#N
INPUT BUFFER UNIT
INPUT BUFFER MEMORY
SCHEDULER
INPUT HW#2
SCHEDULER
INPUT HW#1
#1
#2
#3
#N
OUTPUT HW

FIG.4


NOTIFICATION OF ARRIVAL LINE AND QoS CLASS (TO SCHEDULER)
INDICATION OF READ-OUT LINE(FROM SCHEDULER)
PACKET(CELL)BUFFER(COMMON BUFFER)MEMORY
INPUT HIGHWAY
EXTRACTION OF HEADER
OUTPUT HIGHWAY
WRITE ADDRESS
READ ADDRESS
SELECTION OF READ-OUT QoS CLASS
ADDRESS MANAGEMENT MEMORY
OUTGOING ROUTE#0-0
QoS#0
(16)
QoS#15
ADDRESS
ADDRESS
(128xN)
OUTGOING ROUTE#(N-1)-127
QoS#0
(16)
QoS#15
FREE ADDRESS MEMORY
MULTICAST
QoS#0
(16)
QoS#15

0023801 9956469

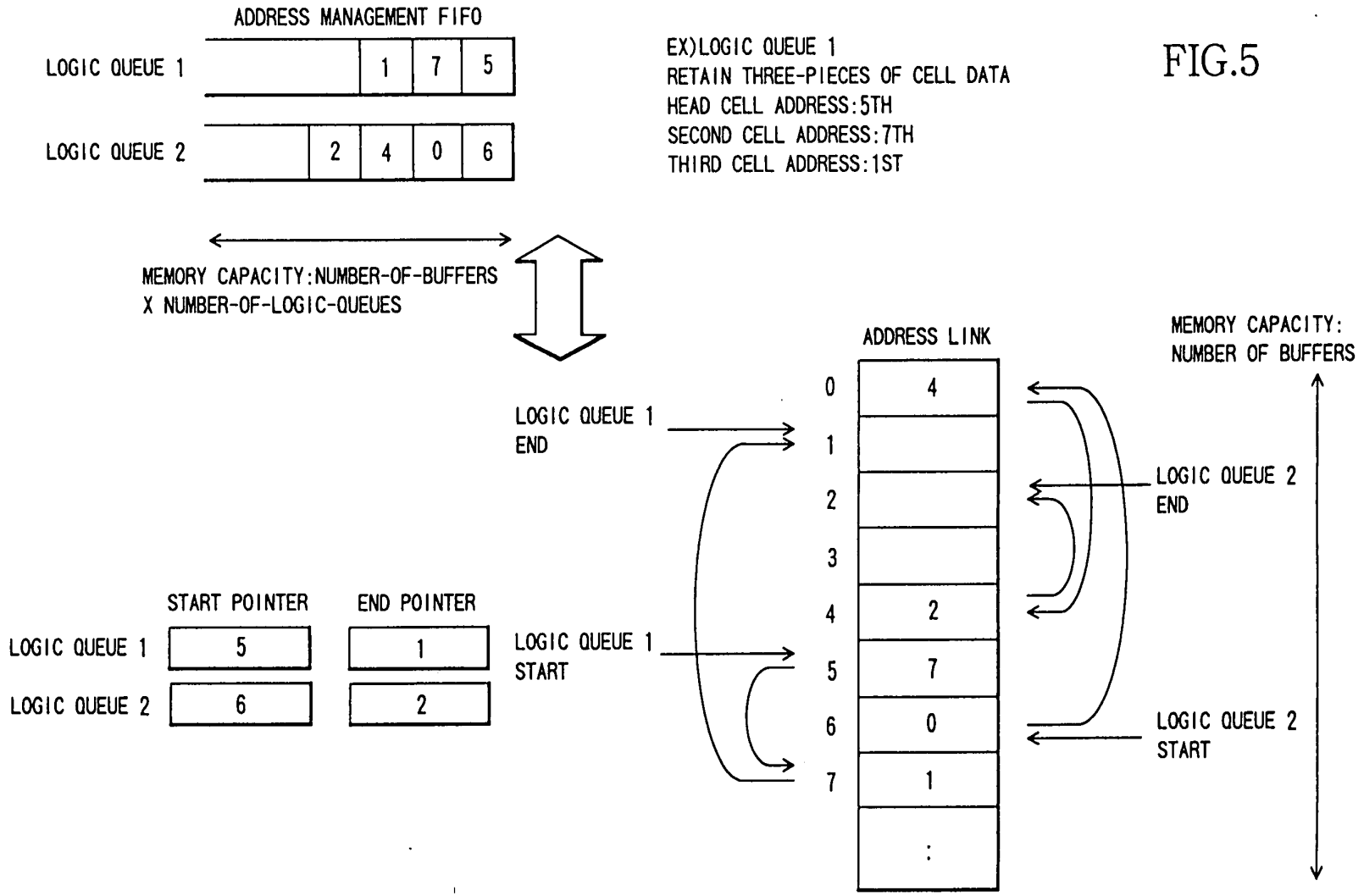


FIG.5

FIG.6

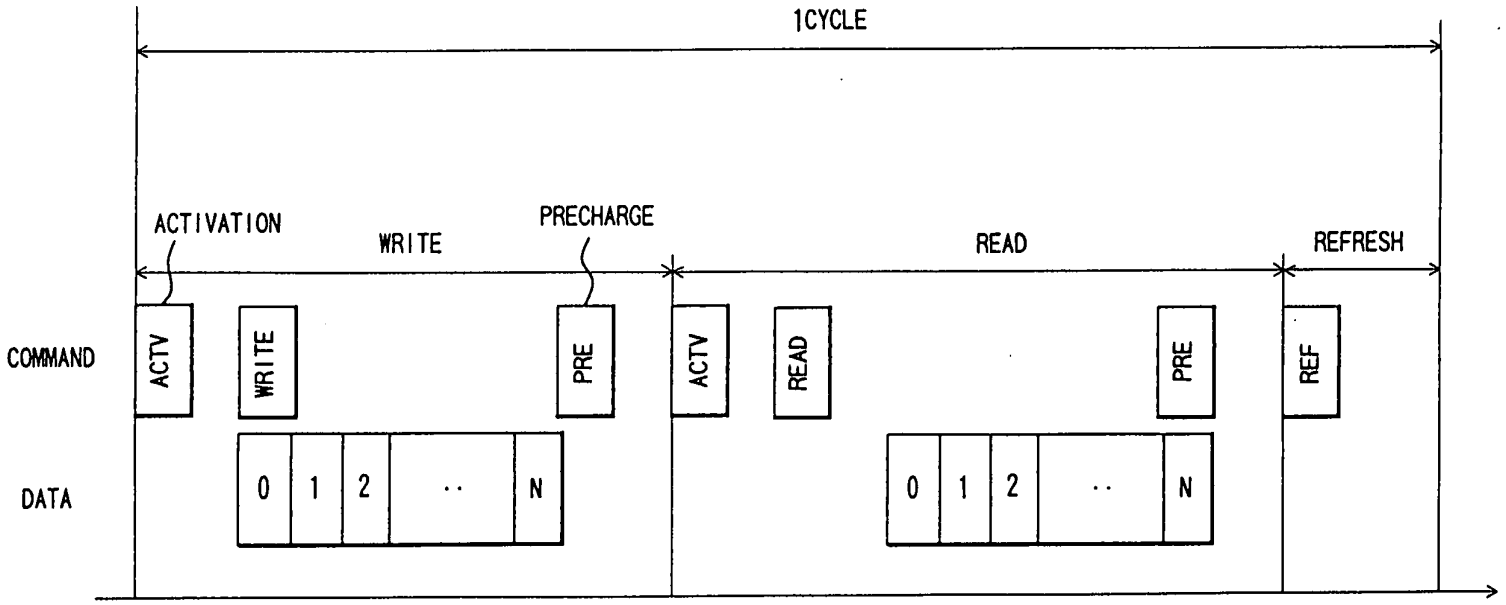

1CYCLE
ACTIVATION
WRITE
PRECHARGE
READ
REFRESH
COMMAND
DATA
ACTV
WRITE
PRE
ACTV
READ
PRE
REF
0
1
2
..
N
0
1
2
..
N

FIG.7

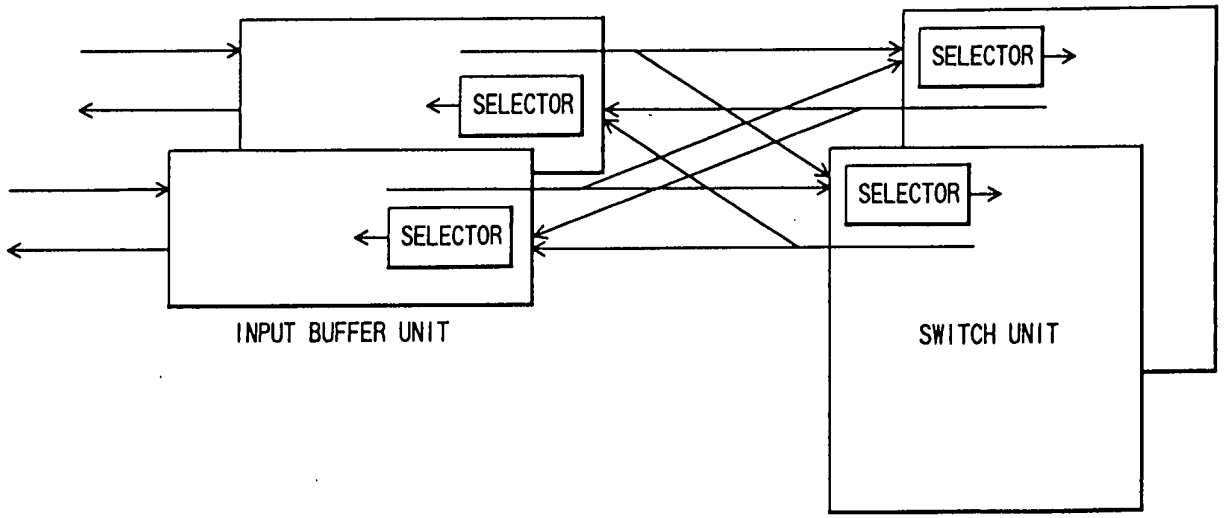
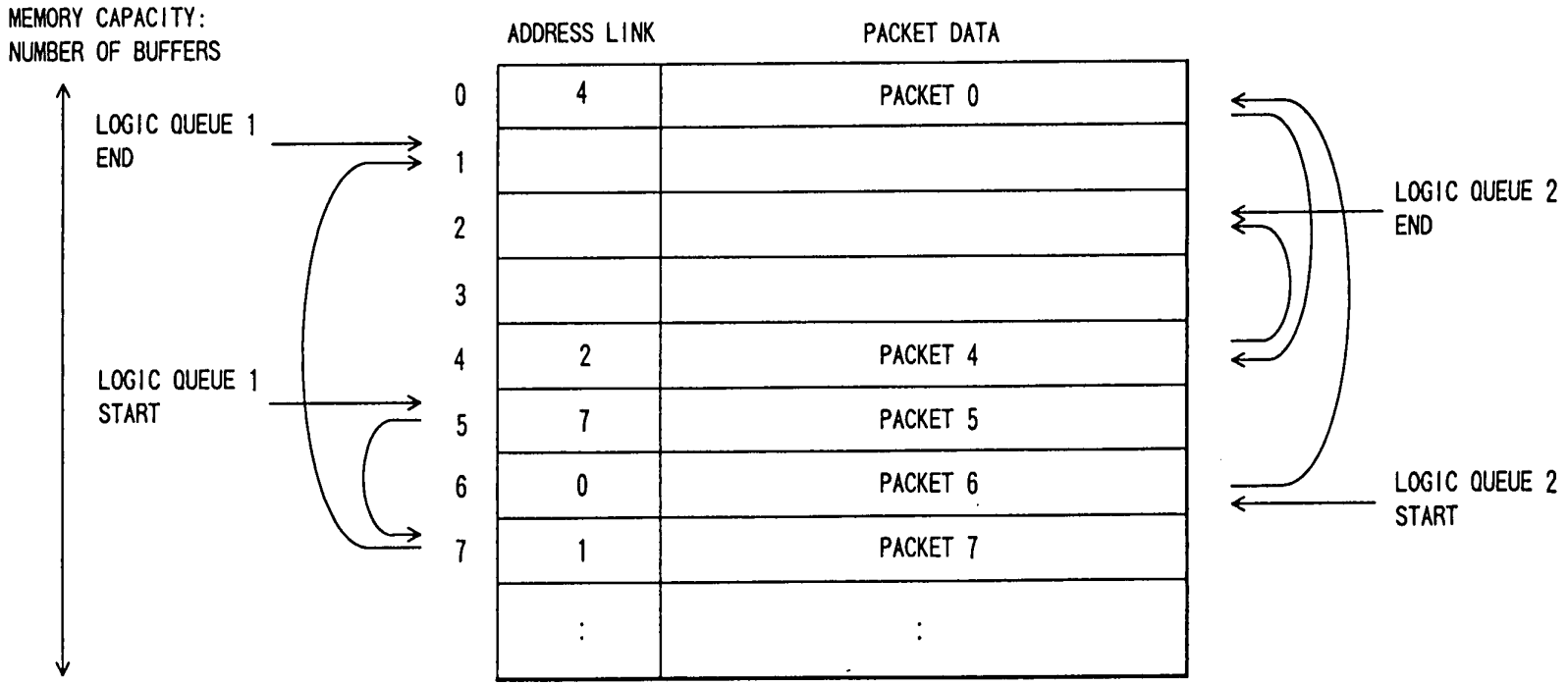

SELECTOR
SELECTOR
SELECTOR
SELECTOR
INPUT BUFFER UNIT
SWITCH UNIT

FIG.8


MEMORY CAPACITY:
NUMBER OF BUFFERS
LOGIC QUEUE 1
END
LOGIC QUEUE 1
START
ADDRESS LINK
PACKET DATA
0
1
2
3
4
5
6
7
4
2
7
0
1
:
PACKET 0
PACKET 4
PACKET 5
PACKET 6
PACKET 7
:
LOGIC QUEUE 2
END
LOGIC QUEUE 2
START

002380"9954960

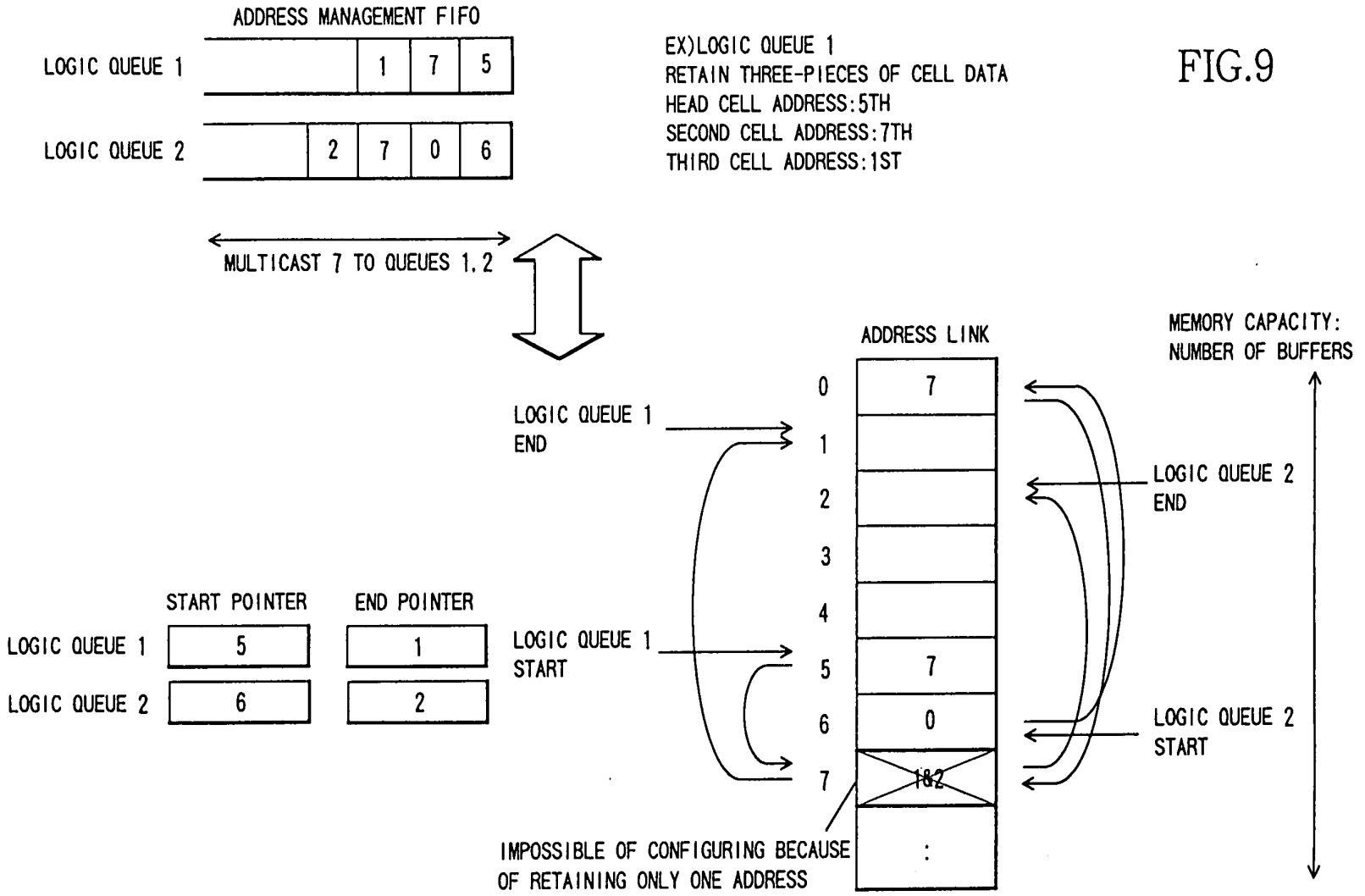


FIG.9

FIG.10

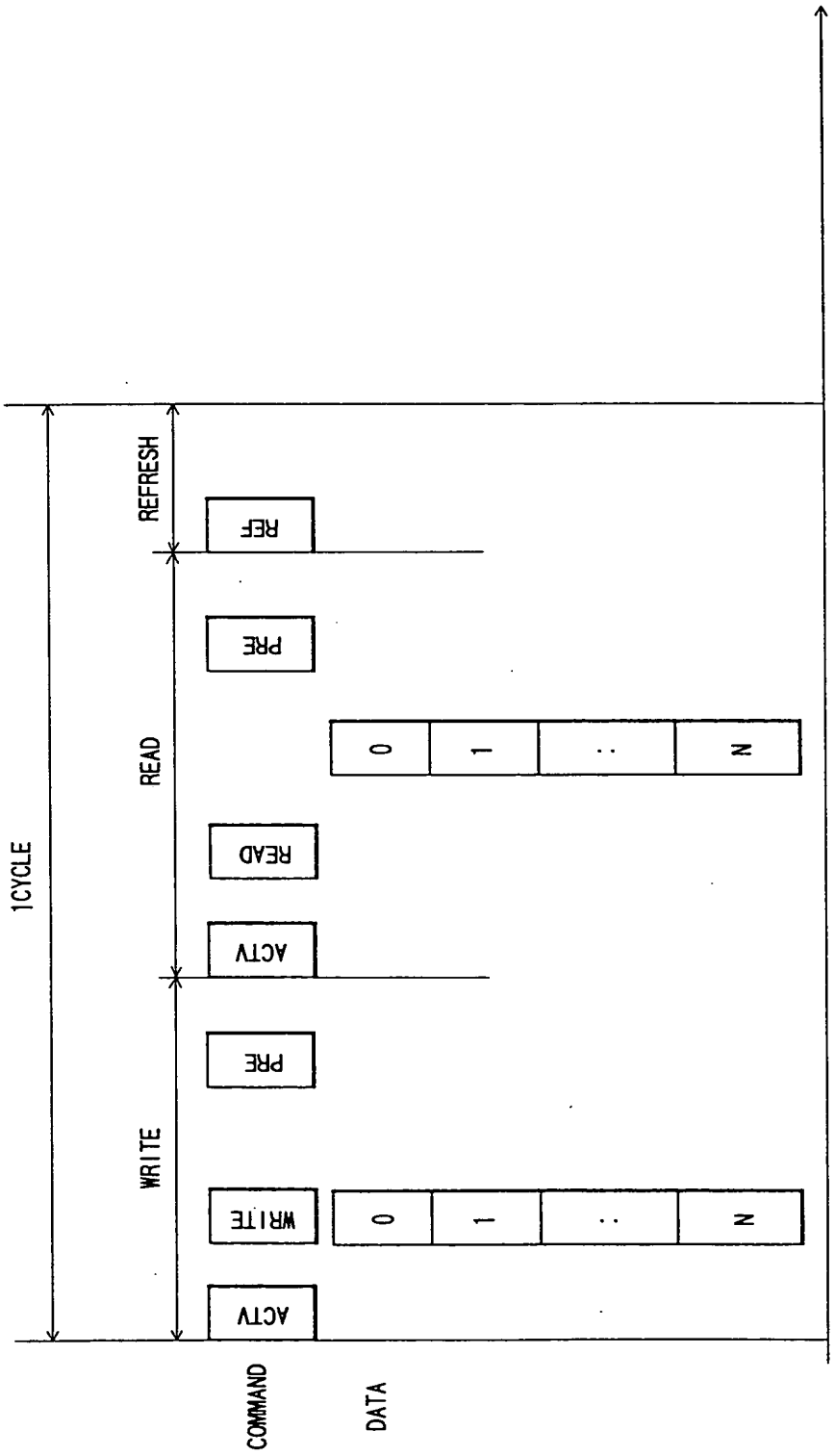

1CYCLE
REFRESH
READ
WRITE
REF
PRE
READ
ACTV
PRE
WRITE
ACTV
0
1
..
N
0
1
..
N
COMMAND
DATA

FIG.11

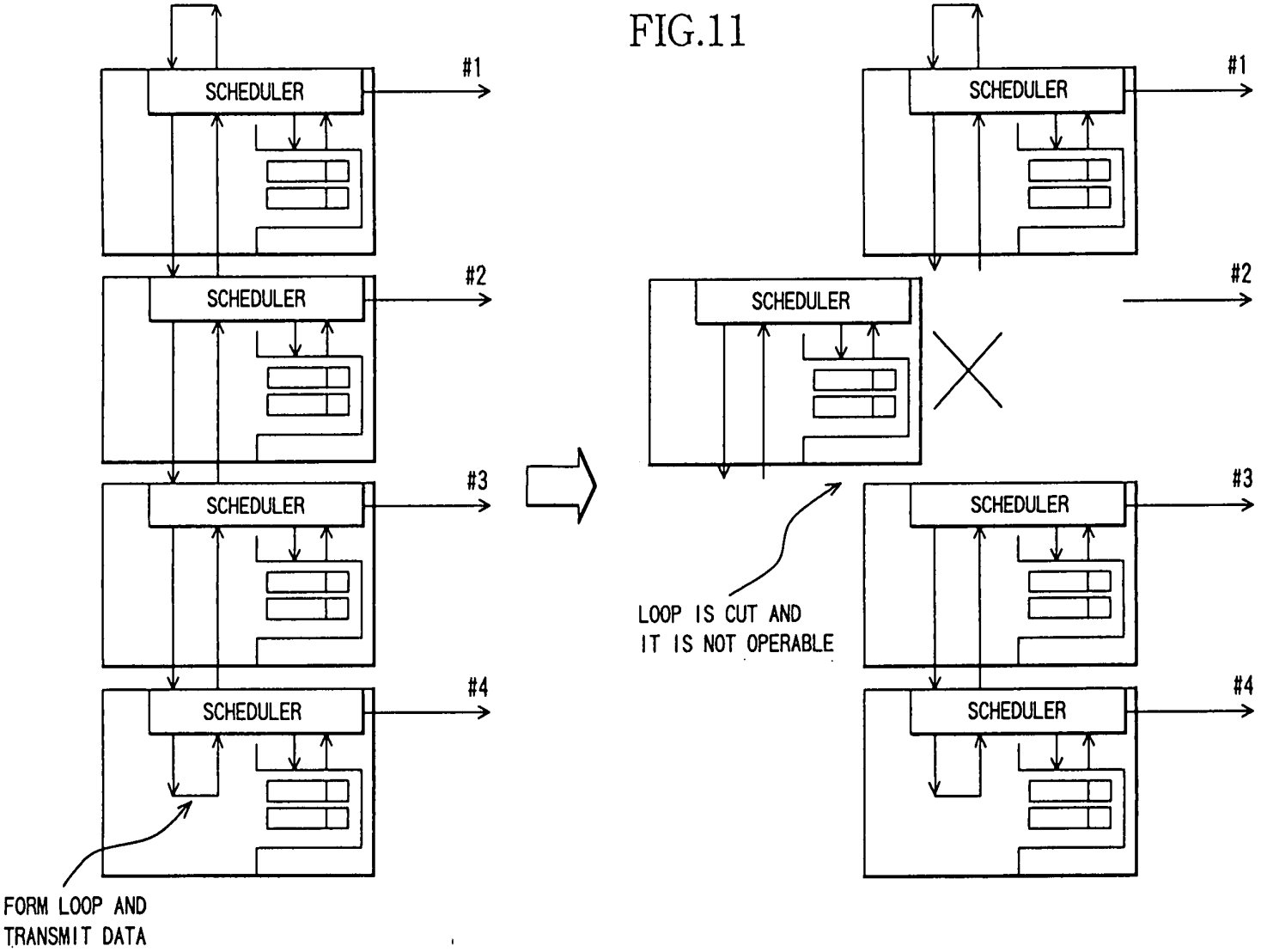

SCHEDULER
#1
SCHEDULER
#2
SCHEDULER
#3
SCHEDULER
#4
FORM LOOP AND
TRANSMIT DATA
SCHEDULER
#1
SCHEDULER
#2
SCHEDULER
#3
SCHEDULER
#4
LOOP IS CUT AND
IT IS NOT OPERABLE

FIG.12

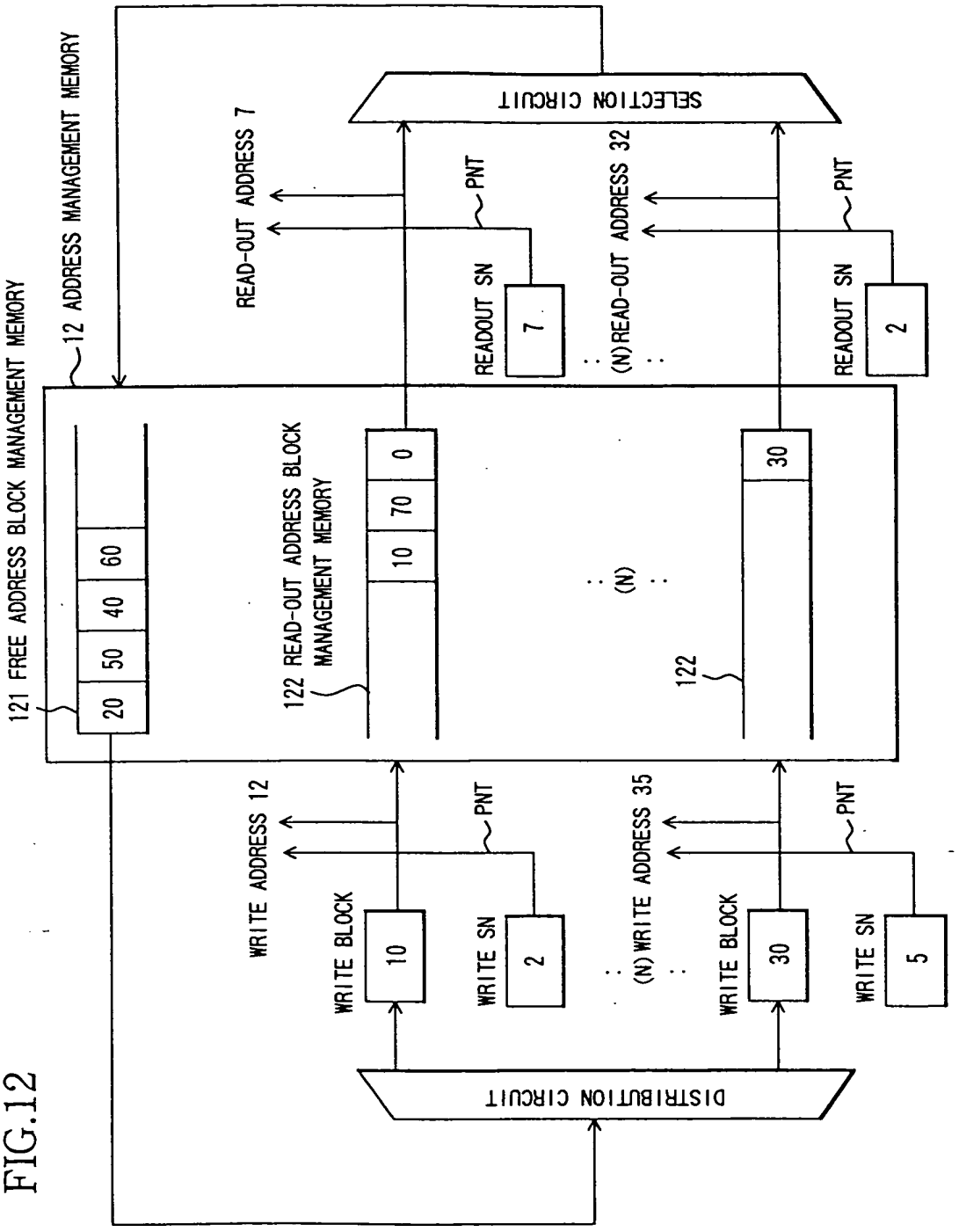

121 FREE ADDRESS BLOCK MANAGEMENT MEMORY
12 ADDRESS MANAGEMENT MEMORY
122 READ-OUT ADDRESS BLOCK MANAGEMENT MEMORY
SELECTION CIRCUIT
DISTRIBUTION CIRCUIT
READ-OUT ADDRESS 7
PNT
READOUT SN
7
(N) READ-OUT ADDRESS 32
PNT
READOUT SN
2
WRITE ADDRESS 12
PNT
WRITE BLOCK
10
WRITE SN
2
(N) WRITE ADDRESS 35
PNT
WRITE BLOCK
30
WRITE SN
5
20
50
40
60
0
70
10
30
(N)
122

FIG.13

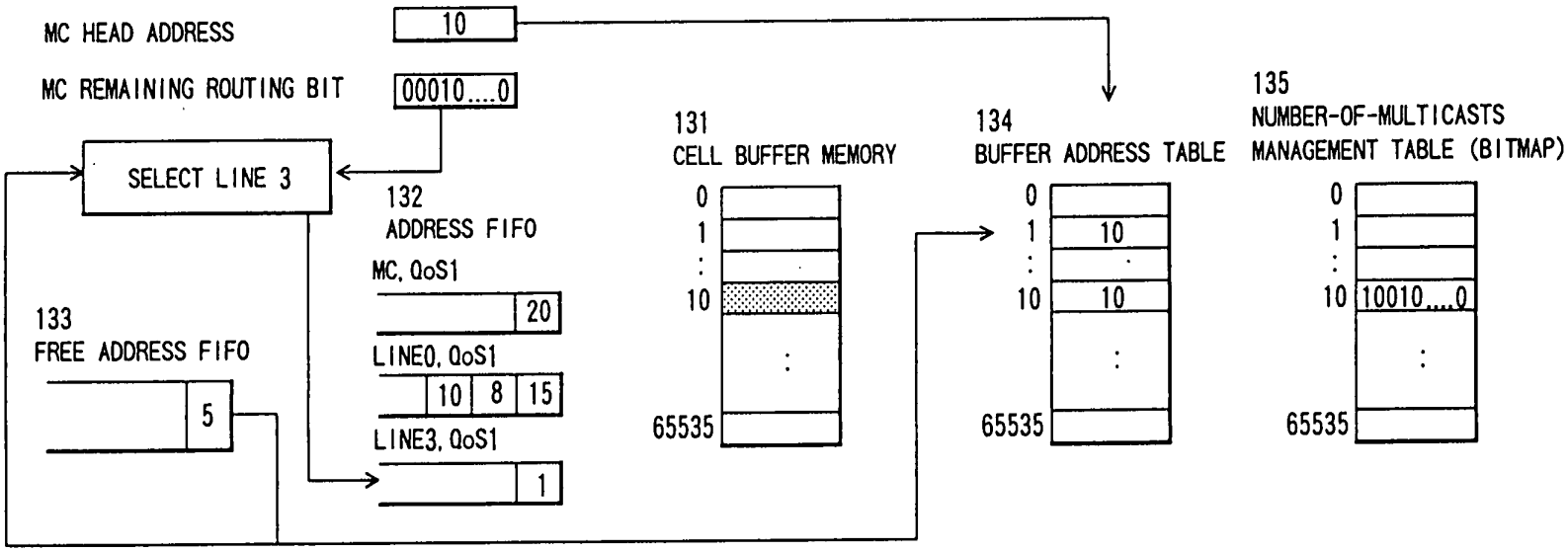

MC HEAD ADDRESS
10
MC REMAINING ROUTING BIT
00010....0
SELECT LINE 3
132
ADDRESS FIFO
MC, QoS1
20
LINE0, QoS1
10
8
15
LINE3, QoS1
1
133
FREE ADDRESS FIFO
5
131
CELL BUFFER MEMORY
0
1
10
65535
134
BUFFER ADDRESS TABLE
0
1
10
10
10
65535
135
NUMBER-OF-MULTICASTS
MANAGEMENT TABLE (BITMAP)
0
1
10
10010....0
65535

FIG.14

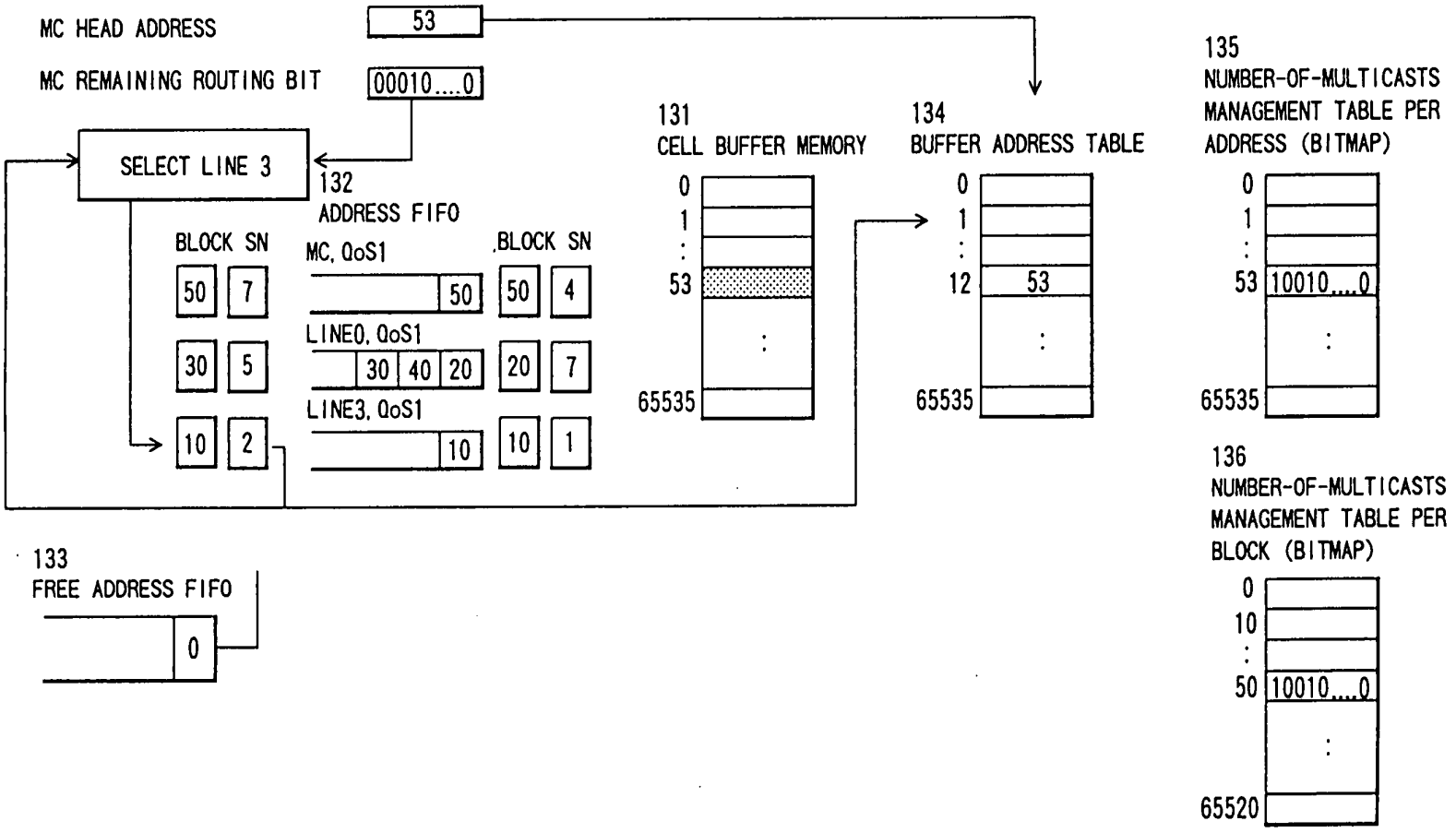

MC HEAD ADDRESS
53
MC REMAINING ROUTING BIT
00010....0
SELECT LINE 3
132
ADDRESS FIFO
BLOCK SN
MC, QoS1
BLOCK SN
50
7
50
50
4
30
5
LINE0, QoS1
30
40
20
20
7
10
2
LINE3, QoS1
10
10
1
131
CELL BUFFER MEMORY
0
1
53
65535
134
BUFFER ADDRESS TABLE
0
1
12
53
65535
135
NUMBER-OF-MULTICASTS MANAGEMENT TABLE PER ADDRESS (BITMAP)
0
1
53
10010....0
65535
136
NUMBER-OF-MULTICASTS MANAGEMENT TABLE PER BLOCK (BITMAP)
0
10
50
10010....0
65520
133
FREE ADDRESS FIFO
0

FIG.15

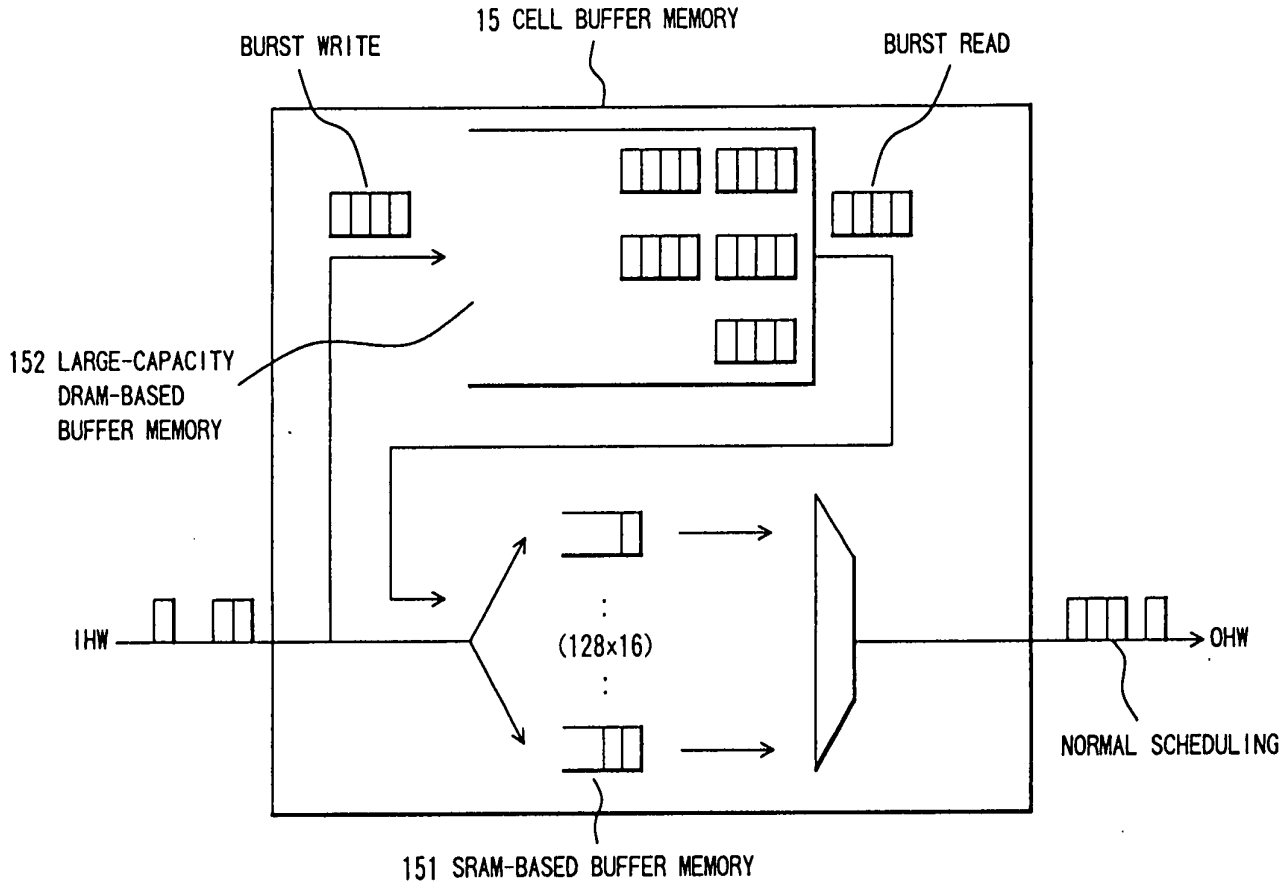

15 CELL BUFFER MEMORY
BURST WRITE
BURST READ
152 LARGE-CAPACITY
DRAM-BASED
BUFFER MEMORY
IHW
(128x16)
OHW
NORMAL SCHEDULING
151 SRAM-BASED BUFFER MEMORY

FIG.16

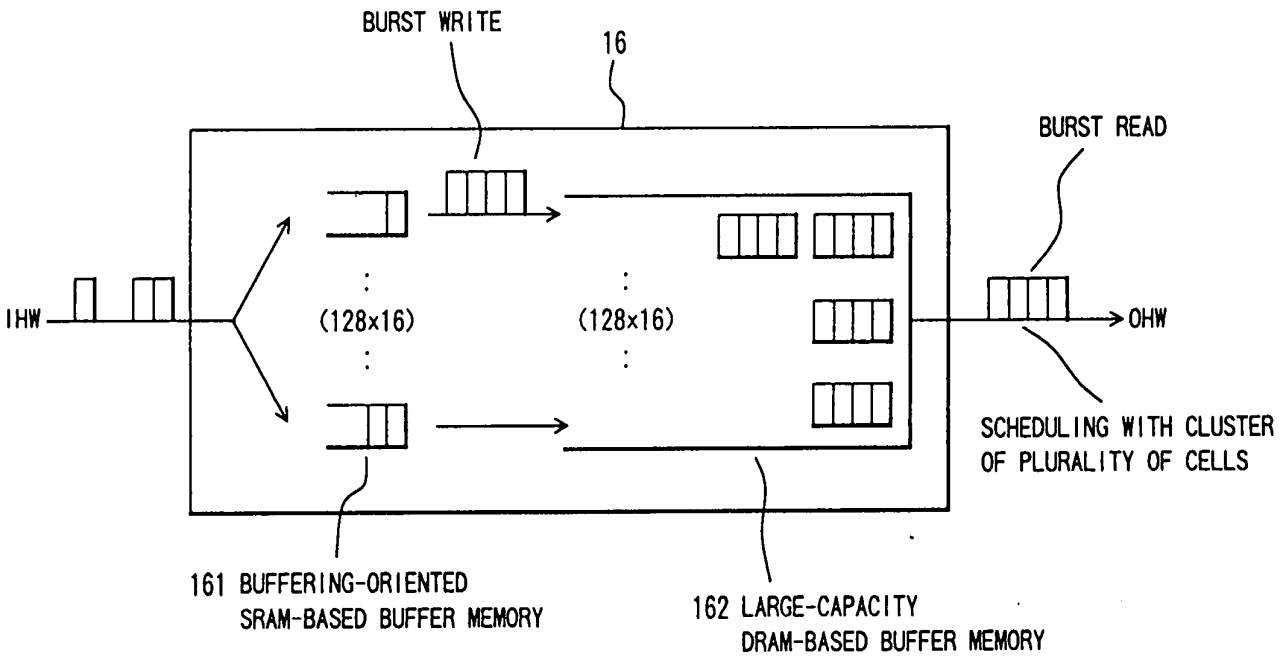

BURST WRITE
16
BURST READ
IHW
(128x16)
(128x16)
OHW
SCHEDULING WITH CLUSTER
OF PLURALITY OF CELLS
161 BUFFERING-ORIENTED
SRAM-BASED BUFFER MEMORY
162 LARGE-CAPACITY
DRAM-BASED BUFFER MEMORY

FIG.17

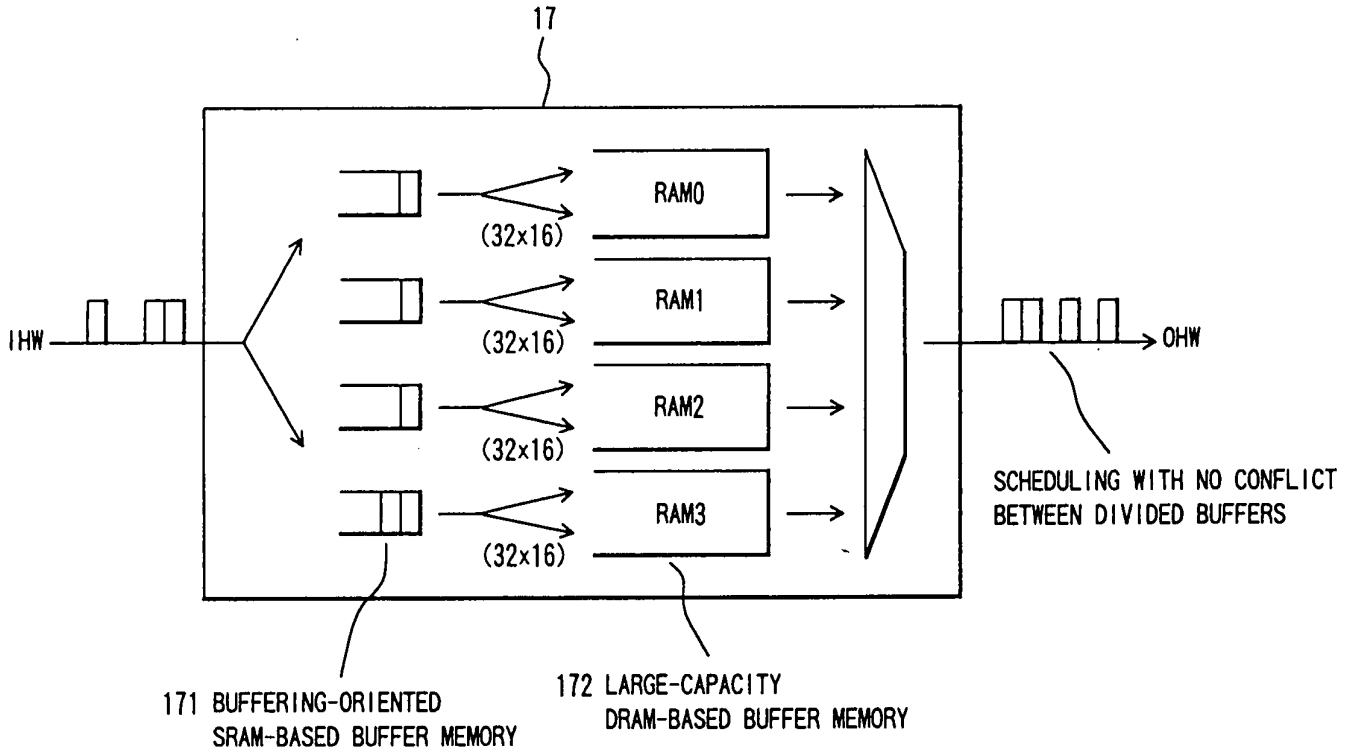

17
RAM0
RAM1
RAM2
RAM3
(32x16)
(32x16)
(32x16)
(32x16)
IHW
OHW
SCHEDULING WITH NO CONFLICT
BETWEEN DIVIDED BUFFERS
171 BUFFERING-ORIENTED
SRAM-BASED BUFFER MEMORY
172 LARGE-CAPACITY
DRAM-BASED BUFFER MEMORY

FIG.18

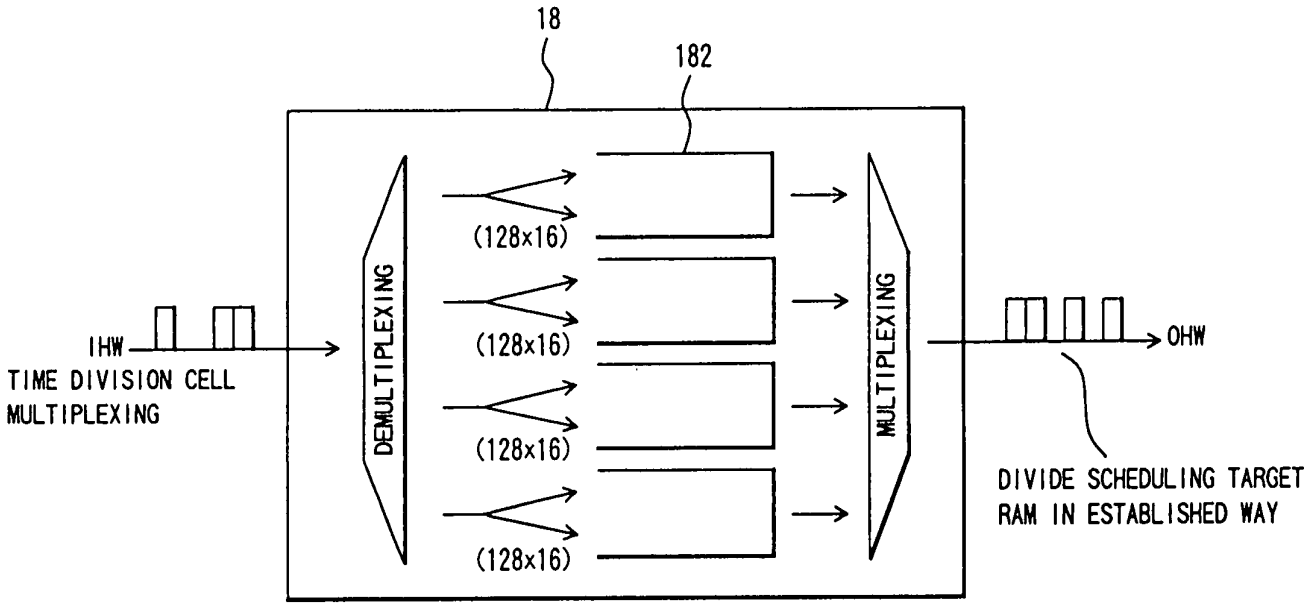

18
182
IHW
TIME DIVISION CELL
MULTIPLEXING
DEMULTIPLEXING
(128x16)
(128x16)
(128x16)
(128x16)
MULTIPLEXING
OHW
DIVIDE SCHEDULING TARGET
RAM IN ESTABLISHED WAY

FIG.19

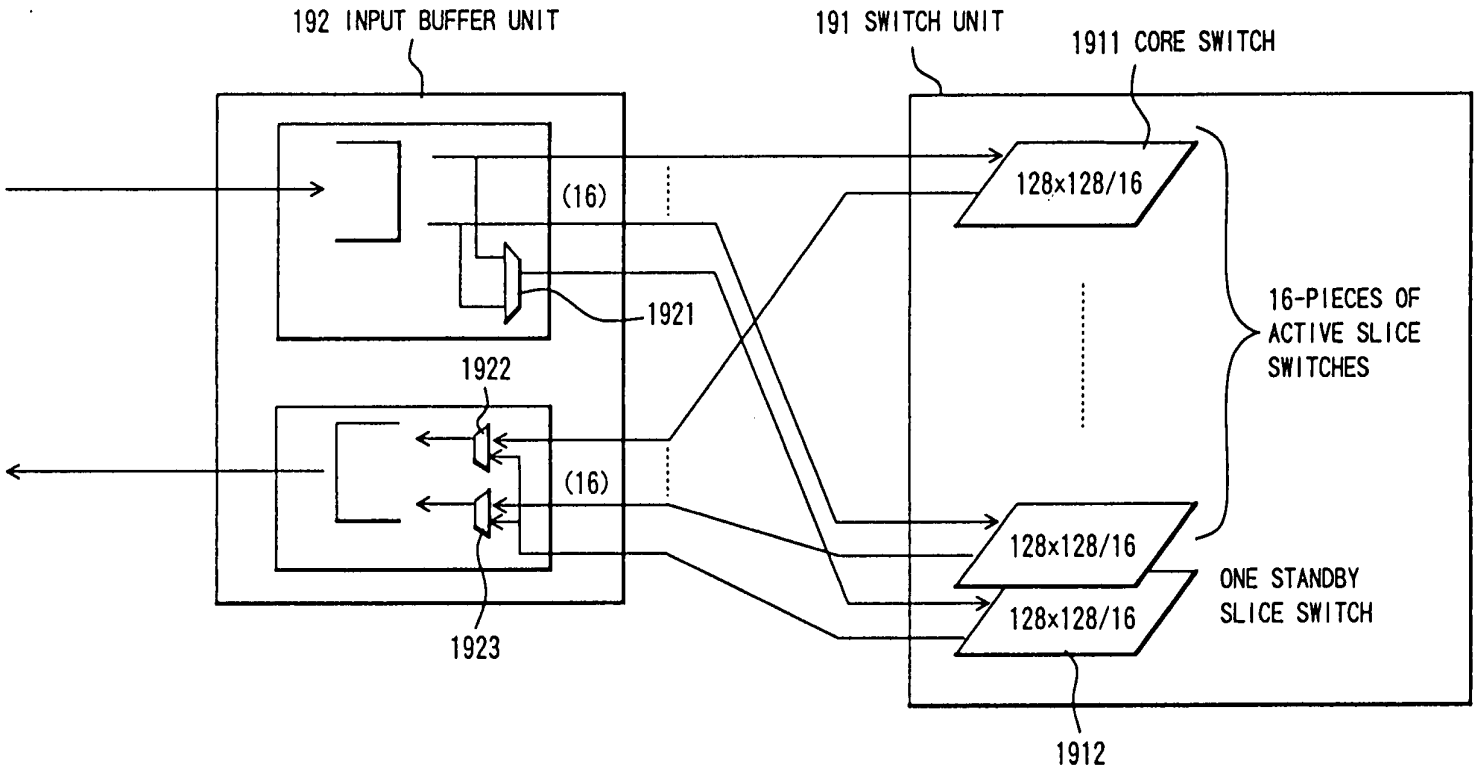

192 INPUT BUFFER UNIT
191 SWITCH UNIT
1911 CORE SWITCH
(16)
1921
1922
(16)
1923
128x128/16
16-PIECES OF
ACTIVE SLICE
SWITCHES
128x128/16
ONE STANDBY
SLICE SWITCH
128x128/16
1912

FIG.20

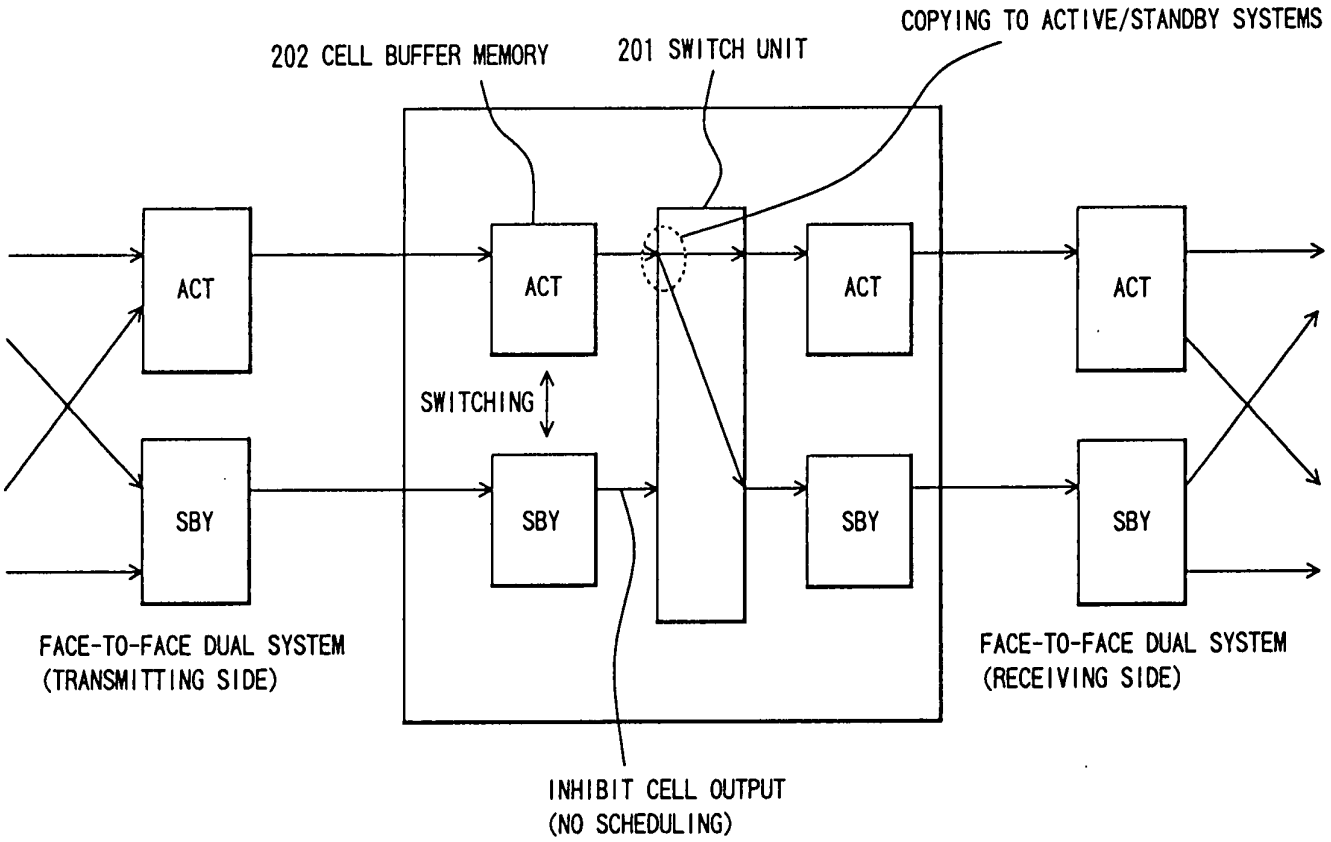

COPYING TO ACTIVE/STANDBY SYSTEMS
202 CELL BUFFER MEMORY
201 SWITCH UNIT
ACT
ACT
ACT
ACT
SWITCHING
SBY
SBY
SBY
SBY
FACE-TO-FACE DUAL SYSTEM
(TRANSMITTING SIDE)
FACE-TO-FACE DUAL SYSTEM
(RECEIVING SIDE)
INHIBIT CELL OUTPUT
(NO SCHEDULING)

FIG.21

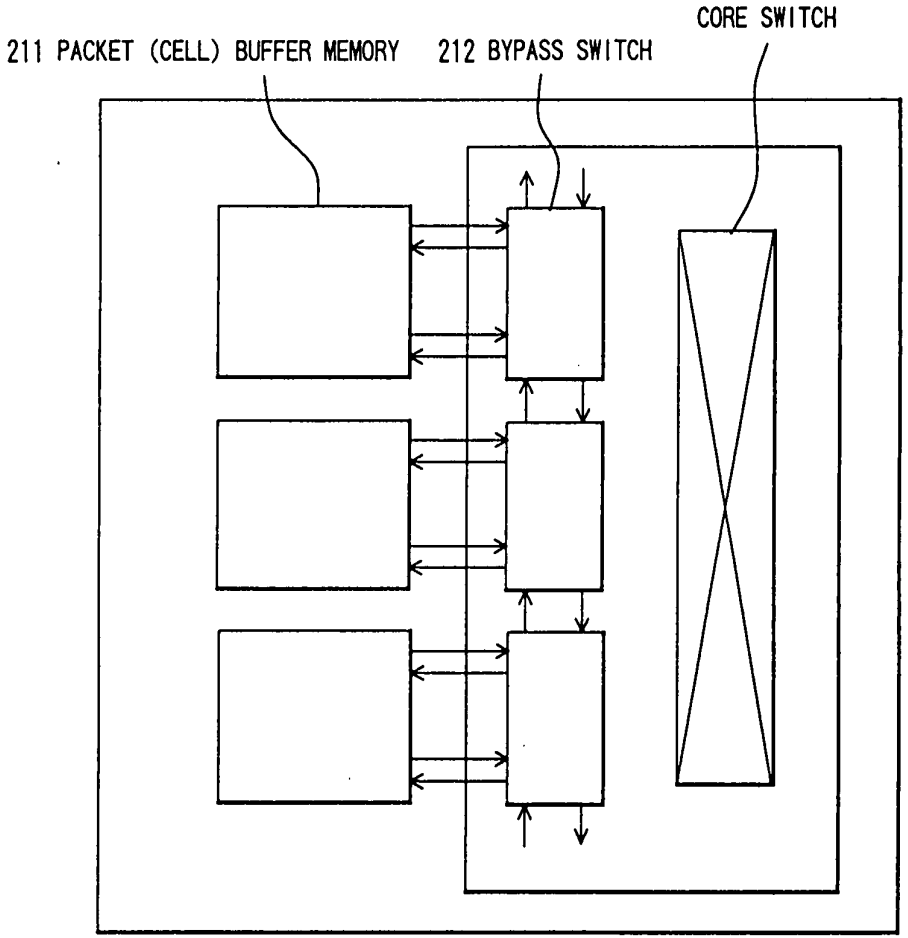
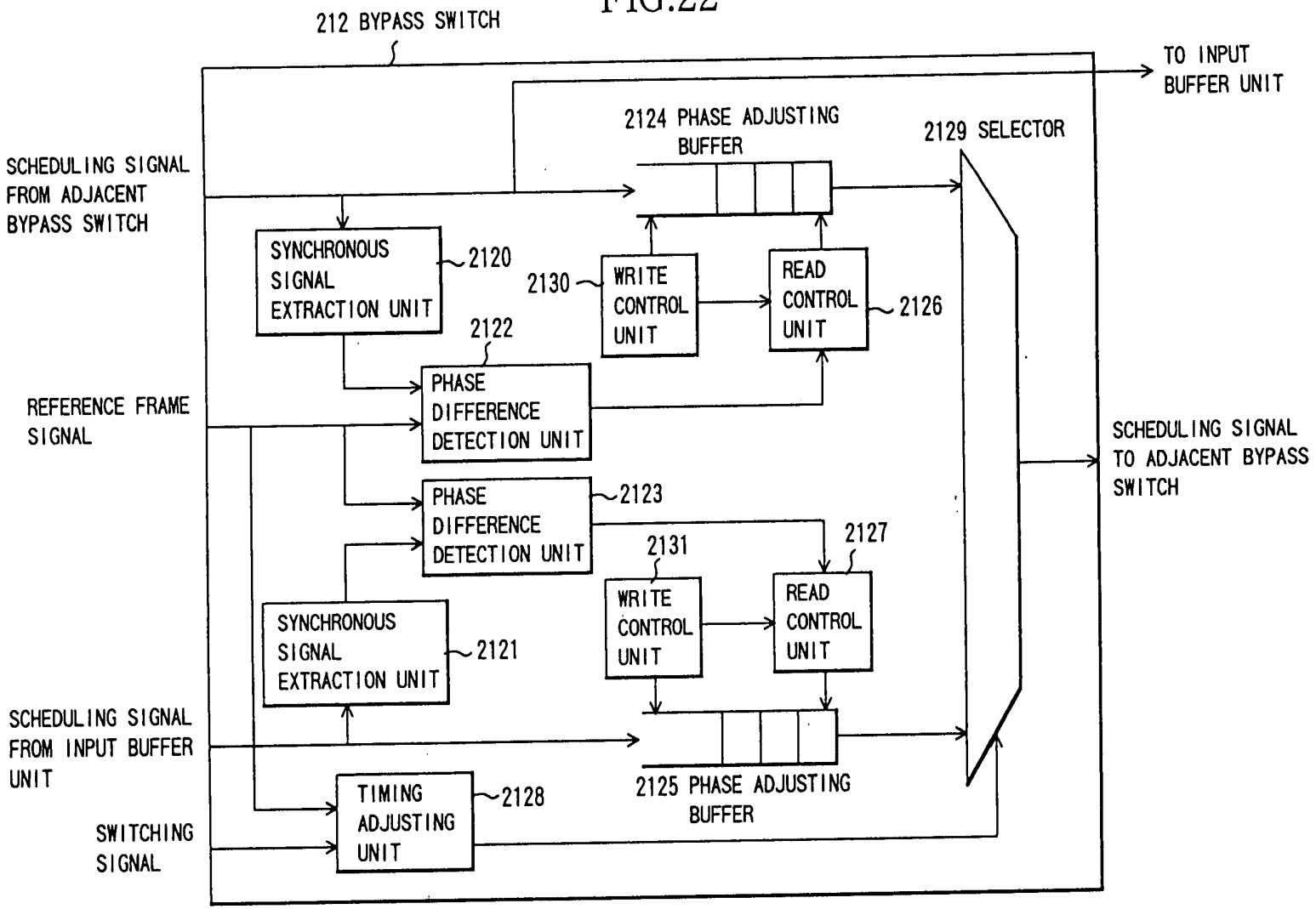

211 PACKET (CELL) BUFFER MEMORY
212 BYPASS SWITCH
CORE SWITCH

FIG.22


212 BYPASS SWITCH
TO INPUT BUFFER UNIT
2124 PHASE ADJUSTING BUFFER
2129 SELECTOR
SCHEDULING SIGNAL FROM ADJACENT BYPASS SWITCH
SYNCHRONOUS SIGNAL EXTRACTION UNIT
2120
2130
WRITE CONTROL UNIT
READ CONTROL UNIT
2126
2122
PHASE DIFFERENCE DETECTION UNIT
REFERENCE FRAME SIGNAL
SCHEDULING SIGNAL TO ADJACENT BYPASS SWITCH
PHASE DIFFERENCE DETECTION UNIT
2123
2131
2127
WRITE CONTROL UNIT
READ CONTROL UNIT
SYNCHRONOUS SIGNAL EXTRACTION UNIT
2121
SCHEDULING SIGNAL FROM INPUT BUFFER UNIT
TIMING ADJUSTING UNIT
2128
2125 PHASE ADJUSTING BUFFER
SWITCHING SIGNAL